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Optoelectronic Packaging and Reliability of Intra- and Inter-board Level Guided-Wave Optical Interconnection

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Optoelectronic Packaging and Reliability of Intra- and Inter-board Level Guided-Wave Optical Interconnection

by

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Optoelectronic Packaging and Reliability of Intra- and Inter-board Level Guided-Wave Optical Interconnection

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Supervisor: Ray T. Chen

We have demonstrated a flexible optical waveguide film with integrated VCSEL and PIN photodiode arrays for the fully embedded board level optical interconnection system. One of the most critical issues in the fully embedded board level optical interconnection system is the signal beam coupling between the guided-wave structure and the aperture of VCSEL (or PIN photodiode). The coupling efficiencies of spherical mirrors are calculated as a function of mirror radius. The optimum mirror radius ranges which are compatible with the fully embedded board level optical interconnection system are theoretically verified.

The thermal characteristics of a thin film VCSEL are studied both theoretically and experimentally. The thermal resistances of VCSEL with variable thickness, ranging from 10 μm to 200 μm, have been determined by measuring the output wavelength shift as a function of the dissipated power. The thermal simulation results agree reasonably well with experimentally measured data. From the thermal management point of view, a

thinned VCSEL has an exclusive advantage due to the reduction of the thermal resistance. The thermal resistance of 10 μm thick VCSEL is 40 % lower than that of 200 μm thick VCSEL. The theoretical analysis of thermal via effects is performed to determine optimized thickness ranges of thin film VCSEL for the fully embedded structure. Thermal resistance of the fully embedded thin film VCSEL with closed and open thermal via structures are also evaluated with the suitable VCSEL thickness reported.

The high-performance computing system is demonstrated using a 16-channel optical backplane using thin film volume holographic gratings. The optical backplane contains TO-46-Can-packaged VCSELs and photodiodes as an optical transmitter and receiver, respectively. Optical packaging plates are fabricated for 4 X 8 array packaging for 16-VCSELs and 16-Photodiodes. Packaging issues including crosstalk and alignment tolerance are studied to design a low cost optical packaging scheme. Thin film volume hologram grating is fabricated on glass substrate to redirect light beams. An individual single channel performs at a 100 MHz data transfer rate. The high-performance computing system using 16-channel optical backplane is demonstrated at a 1.6 Gbps data transmission.

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Chapter 1: Introduction

Due to the rapid and wide expansion of the internet service, every personal computer is now connected to every other computer all over the world. The number of computers and servers connected with the web has increased every year. The amount of data also increased because large amounts of data can be handled by the increased executive speed of the central process unit (CPU).

The most recent International Technology Roadmap for Semiconductors (ITRS) projects that while per-chip performance will continue to improve at a rate of approximately four times every three to four years, the number of signal pins per module will only double over the same period, and the maximum bit rate per signal pin will increase by only 35% [1]. Fig. 1-1 shows the history of computer Input/Output (I/O) protocols and the corresponding signalling rates in copper interconnects on Printed Circuit Boards (PCBs) [2]. By 2010, the requirement of the off-chip clock frequency will reach more than 12 GHz. Also, modern multiprocessor computer architectures place stringent demands on the inter processor connection network. Thus, the total off-chip I/O bandwidth, pin count times bit rate per pin, will increase by roughly 2.7 times, while the internal chip performance improves by four times [3]. However, the computing performance is not proportional to the number of processors. In a typical system, processors and memory are distributed across several different nodes, and data must be constantly transferred between them as computing operations occur. The performance of

multiprocessing systems is mainly limited by the bandwidth and delay of electrical interconnections.

Optical interconnection technology should become more important in the near future, because the electrical interconnection is limited by speed and the difficulty of high integration density. At a high frequency operation (>12 GHz), copper transmission lines on PCB provoke degradation in the rise and fall times of electrical signals as mentioned previously.

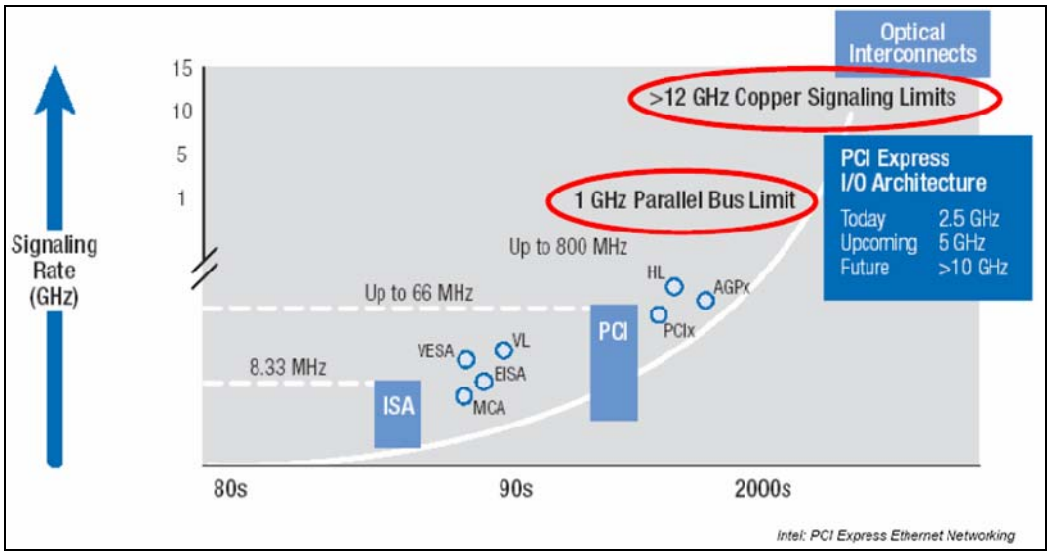


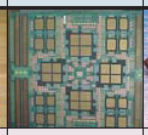
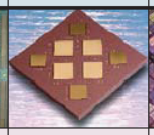
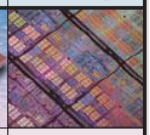
Figure 1-1 Computer I/O architecture history and I/O roadmap [Intel Technology Journal, Vol. 8, Issue 2, pp 115~127, 2004]

Advantages in the characteristics of optics in communication systems, as compared to conventional electronics, have led to a widespread replacement of copper wires for communication at data rates above Mbps and over kilometers. Today optical communication systems are used in many applications such as synchronous digital

hierarchy (SDH) / synchronous optical network (SONET) systems, wavelength division multiplexing (WMD) network systems, Metropolitan Area Networks (MANs), Local Area Networks (LANs), Fiber-to-the-Home (FTTH) and board-to-board interconnections, all of which utilize optical fiber as the means of conveying data [4,5].

Table 1-1 shows the physical interconnect hierarchy. Optics has been used for longer-distance links for several decades, with progressively less use of optics for shorter links. Currently, for bit rates in the range of 1 ~ 10 Gbps, optical technologies are in common use for links longer than a few meters [3].

Table 1-1 Sever Physical Interconnection Hierarchy [*IBM J. RES. & DEV.*, Vol. 49, No. 4/5, pp755~775, July 2005]

	MAN/WAN	Cables–long	Cables–short	Card-to-card	Intra-card	Intra-module	Intra-chip
							
Length	Multi-km	10–300 m	1–10 m	0.3–1 m	0.1–0.3 m	5–100 mm	0–20 mm
No. of lines per link	One	One to tens	One to tens	One to hundreds	One to hundreds	One to hundreds	One to hundreds
No. of lines per system	Tens	Tens to thousands	Tens to thousands	Tens to thousands	Thousands	Approximately ten thousand	Hundreds of thousands
Standards	Internet Protocol, SONET, ATM	LAN/SAN (Ethernet, InfiniBand, Fibre Channel)	Design-specific, LAN/SAN (Ethernet, InfiniBand)	Design-specific and standards (PCI, backplane InfiniBand and Ethernet)	Design-specific, generally	Design-specific	Design-specific
Use of optics	Since the 1980s	Since the 1990s	Present time, or very soon	2005–2010 with effort	2010–2015	Probably after 2015	Later

To overcome the bottlenecks in today's electronics related to the high-density packaging of copper transmission lines, one possible solution is to use optical backplanes and PC-boards based on (planar polymer) optical waveguides, because these are far less sensitive to EMI than electrical interconnects [6].

Various ideas on optical interconnection techniques are applied to overcome the frequency dependent loss of electrical interconnection lines [7]–[9]. Table 1-2 shows the summary of research activities in the world on the optical interconnections for shorter links. Although there was a significant worldwide research interest over the past 15 years on optical inter/intra chip interconnect and optical PC-boards and backplanes, a product has not succeeded on the market until now.

Table 1-2 Global Research Activities on the Board Level Optical Interconnection.

Global Research Groups		References
- Ghent University	Belgium	[10]
- Asperation Oy - Helsinki University of Technology - VTT Electronics	Finland	[11],[12] [13],[14] [15],[16]
- University of Ulm & Daimler Chrysler AG - Dortmund University	Germany	[17] [18]
- IBM Zürich - Swiss Federal Institute of Technology	Switzerland	[19]
- Heriot-Watt University	Great Britain	[7]
- Electronic and Telecommunication Research Institute(ETRI) - Information and Communication University	South Korea	[20],[21] [22]
- Industrial Technology Research Institute (ITRI)	Taiwan	[23]
- Intel Corporation - Duke University (Durham, NC) - Georgia Tech (Atlanta, GA) - ***University of Texas (Austin)***	United States	[27] [24],[25] [26] [28],[29],[30],[31]

Huang *et al.* [32] point that, although the viability of technical solutions has been published, hardly a concept for their use in a computer system can be found in the literature. Furthermore, the cost of replacing electrical links with optical links must be reduced to make optics competitive in high-speed and high-density applications from a market point of view. Lukowicz *et al.* [7] reasoned in a similar way and named inadequate and costly packaging technology and inadequate system architecture as the reasons for the small impact of optical interconnections on board or rack level in real-life systems.

As mentioned previously, the optical interconnections have great advantages compared to the electrical interconnections. However, the reliability of these systems due to packaging vulnerability is one of the paramount concerns. To relieve packaging difficulty, we have developed the fully embedded board-level optical interconnection system [28~31]. All the optoelectronic components including VCSEL array, PIN photodiode array, TIR coupling mirror and planar polymer waveguides are integrated within the 3-D interconnection layers during the conventional PCB fabrication processes. A 12-channel 850 nm GaAs VCSEL array is employed to convert electrical signals to optical signals. Optical signals are transmitted through a 12-channel polymer waveguide array and then converted to electrical signals by a 12-channel GaAs PIN photodiode array. Through the micro-via structures, electrical signals and bias are transmitted from electrical layer to embedded optical layer and vice-versa.

To verify the optimum shape of micro-mirror structures for a fully embedded optical interconnection system, theoretical studies are performed to calculate the coupling

efficiencies as a function of radius of quarter-sphere shape micro-mirror structures. Also the fabrication processes of 12-channel polymer waveguides including 45^{o} micro-mirror structure are described.

In this architecture, however, the self-heating effect of the vertical-cavity surface-emitting laser (VCSEL) cause critical issues in the system reliability since integrated VCSEL arrays are surrounded by thermal insulators such as optical polymer films(TOPAS®) and PCB bonding materials (prepreg or pressure-sensitive-adhesive film). Because the operating lifetime of VCSEL decreases exponentially with temperature, the thermal reliability of the embedded VCSEL arrays is one of the prime concerns in the fully embedded optical interconnection system.

This dissertation presents theoretical and experimental studies of the thermal characteristics of the fully embedded thin film VCSEL array which determines the effective thermal via structures. Thermal resistances as a function of the substrate thickness of VCSEL are experimentally measured. 2-D finite-element analysis is performed to simulate the temperature field distribution near and across the active region inside VCSEL as a function of the substrate thickness of VCSEL and the thermal via structure. Not only the heat generation in the active region but also the joule heating (I^2R) effect in the distributed Bragg reflectors (DBRs) are considered by the thermal-electric direct coupled-field analysis.

Optical backplane uses an optical signal to realize communications for board-to-board interconnection. Each board is equipped with optoelectronic converters (VCSELs and photodiodes) for the emission and detection of modulated optical signals. Several

optical bus architectures based on the optical backplane have been proposed including the substrate-mode guided-wave bus system implemented with wave-guiding plates and holographic grating elements [33,34,35] and the free-space bus systems implemented through free-space optical interconnections [36,37].

In this dissertation, a three-dimensionally interconnected 16-channel optical backplane is demonstrated for a high-performance computing system. The optical backplane contains TO-46-CAN-packaged VCSELs and photodiodes as an optical transmitter and receiver, respectively. Thin film volume holographic gratings are fabricated to refract light beams into a glass wave-guiding plate (n = 1.52) for total internal refraction. Through the VHOE (Volume Holographic Optical Elements), equalized fan-out beam intensities are experimentally measured.

Packaging issues including crosstalk and alignment tolerance are theoretically studied to design low cost and simple optical packaging structure. A 4 X 8 optical packaging plate is fabricated to assemble 16-VCSELs and 16-Photodiodes. VCSELs and photodiodes are inserted alternatively into 32-holes, drilled with 4 X 8 row-and-column pattern, on the packaging plate. VCSEL driver ICs and TIAs (trans-impedance amplifiers) for photodiode are integrated on the PC-board to control VCSEL and to amplify electrical signals from photodiodes, respectively. A 1.6 Gbps of data transmission rate (100 Mbps per single channel) is demonstrated through the optical backplane system using volume holographic gratings.

1.1. Dissertation Outline

This dissertation includes the results of novel designs and fabrication of the fully embedded board level optical interconnect and the 16-channel optical backplane bus using volume holographic optical elements (VHOE). The first 3 parts (Chapter 2, 3 and 4) of this dissertation is dedicated to the design and fabrication of the fully embedded board level (intra-board level) optical interconnection system and the electro-thermal characterization of thin film VCSEL. The second part (Chapter 5) presents the design and fabrication of the 16-channel optical backplane bus (inter-board level) with volume holographic gratings for high performance computing system. A brief chapter-to-chapter outline of the dissertation is given below.

Chapter 2 provides fabrication and characterization of the fully embedded chip-to-chip optical interconnection system. At the first section, the fully embedded board level optical interconnection system is introduced and the fabrication processes of 12-channel polymer waveguides including 45^{o} micro-mirror structure are described. 20 μm thick thin film VCSEL and PIN photodiode arrays are fabricated and electrical/optical properties are characterized.

Chapter 3 introduces the optimum shape of micro-mirror structures for a fully embedded optical interconnection system. Theoretical studies are performed to calculate the coupling efficiencies as a function of radius of quarter-sphere shape micro-mirror structures.

Chapter 4 describes the thermal reliability of thin film VCSEL for the fully embedded chip-to-chip optical interconnection system. The first section of this chapter

covers the fabrication process of thin film VCSEL and the integration techniques to form optical film layer including thin film VCSEL/PD and polymer waveguides. The coupled field electro-thermal simulation module of the ANSYS software is used to calculate thermal resistance of thin film VCSEL as a function of thickness. Some electro-thermal measurement results are also included. At the time of this writing, the heat generation mechanism of VCSEL is discussed and the relationship between the optimum VCSEL thickness and thermal via dimension for the fully embedded structure are studied.

Chapter 5 describes the design and fabrication of a multi-channel optical backplane bus system for a high performance computing system. Thin film volume holographic gratings are fabricated to refract light beams into a glass wave-guiding plate for total internal refraction. Through the VHOE (Volume Holographic Optical Elements), equalized fan-out beam intensities are experimentally measured. Packaging issues including crosstalk and alignment tolerance are theoretically studied to fabricate a novel optical packaging structure. A 4 X 8 optical packaging plate (row-and-column pattern) is fabricated to assemble 16-VCSELs and 16-Photodiodes. VCSEL driver ICs and TIAs (trans-impedance amplifiers) for photodiodes are integrated on the PC-board to control VCSELs and to amplify electrical signal from photodiodes, respectively. Multi-channel data processing with a 1.6 Gbps data transmission rate (100 Mbps per single channel) is successfully demonstrated through optical backplane bus system using VHOE.

Chapter 2: Fabrication and Implementation of Fully Embedded Chip-to-chip Guided-wave Optical Interconnection System

2.1. Fully Embedded Chip-to-chip Guided-Wave Optical Interconnection

To relive package difficulties of optical components and ensure compatibility with a conventional printed circuit board (PCB) lamination process, a fully embedded board level optical interconnection system was introduced [28][29][30][31]. The critical components of the fully embedded board-level optical interconnection system are a vertical cavity surface emitting lasers (VCSEL) array, polymer-based channel waveguides including surface-normal couplers, and a PIN photodiode array. Fig. 2-1 shows schematic diagrams of a fully embedded structure. During the conventional PCB fabrication processes, an optical film layer including VCSEL array, PIN photodiode array, TIR coupling mirror and planar polymer waveguides is integrated within the 3-D interconnection multi-layers. A 12-channel 850 nm GaAs VCSEL array transfers electrical signals to optical signals. Optical signals are transmitted through a 12-channel polymer waveguide array and then transferred to electrical signals by a 12-channel GaAs PIN photodiode array.

The driving electrical sources to modulate the VCSEL and the demodulated electrical signals received from PIN photodiode flow through micro-via structures connected from the surface of the PCB. The fully embedded board-level optical interconnection structure makes the insertion of optoelectronic components into microelectronic systems much more realistic when considering the fact that the major

stumbling block for implementing optical interconnection onto high performance microelectronics is the packaging incompatibility. All the real estates on the PCB surface are occupied by electronics not by optoelectronic components. Therefore, the performance enhancement due to the employment of the optical interconnection is observed and there is no interface problem between electronic and optoelectronic components.

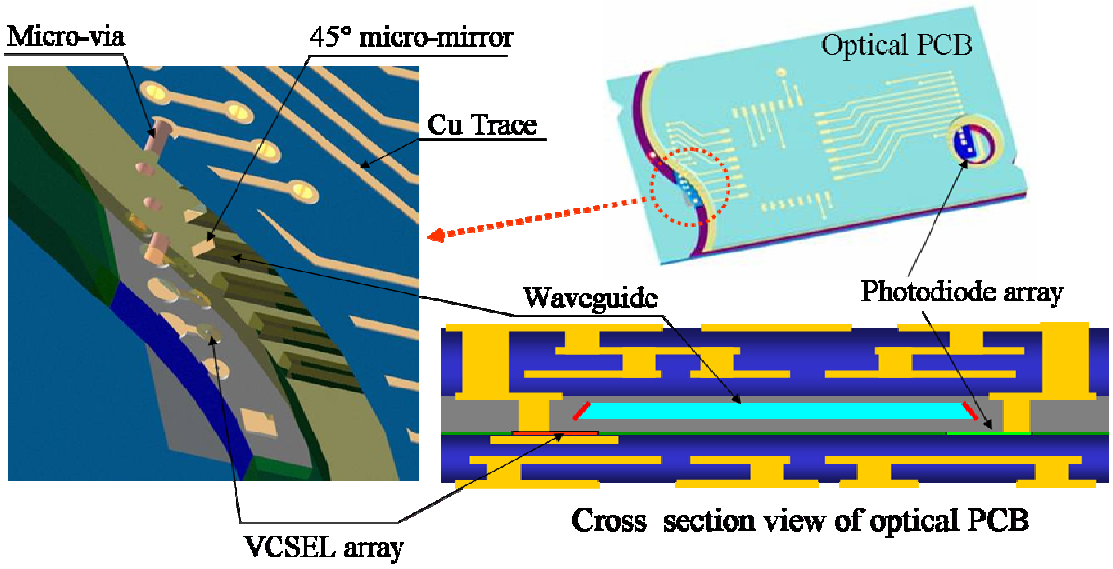
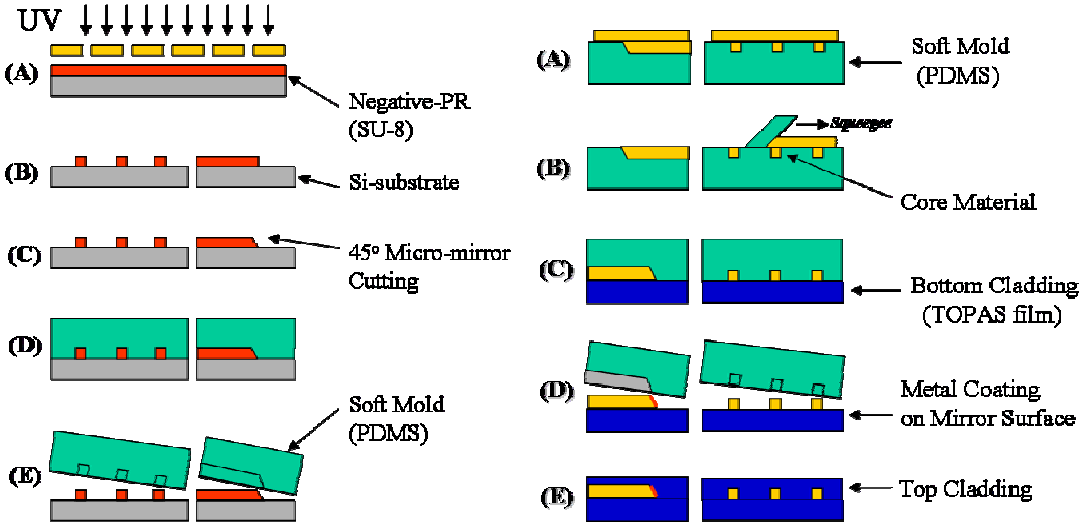


Figure 2-1 Schematic diagrams of the fully embedded board-level optical interconnection system

2.2. Fabrication of 12-channels Polymer-based Waveguides and 45° Micro-Mirror Structures

A Polymer-based 12-channel optical waveguide film is fabricated by the soft molding process [31]. For the soft molding process, first, the soft mold is fabricated. Fig.

2-2 describes (1) the fabrication steps for the soft mold and (2) the soft molding processes.



<Soft-mold fabrication steps> <Soft-molding Processes>

Figure 2-2 Fabrication steps for 12-channel polymer-based waveguide film by the soft-molding processes

To fabricate the soft mold, the master waveguide structures are constructed on a silicon wafer using a standard photo-lithography process. The negative type photo-resist, SU8-2050 (MicroChem^{TM}) is used as a material of the master waveguide structures. As shown in Fig. 2-3, a 12-channel waveguide structure is fabricated on the 6" silicon wafer and each channel has a square shape (50 μm X 50 μm) cross-section.

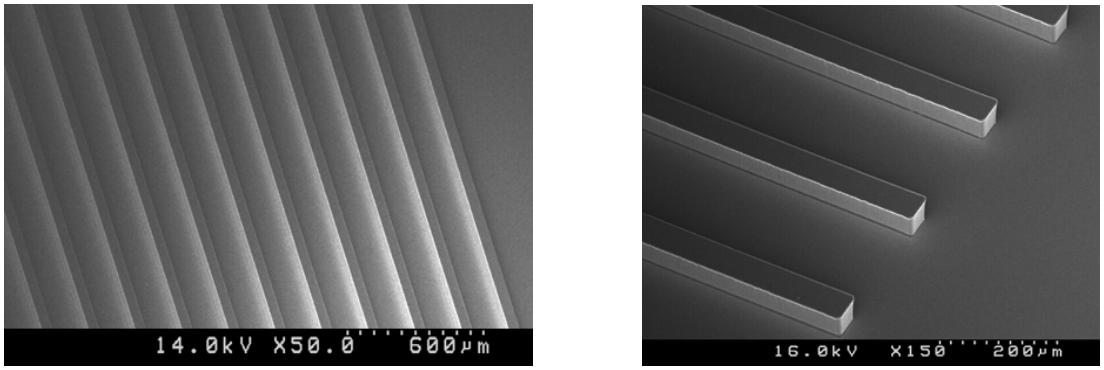
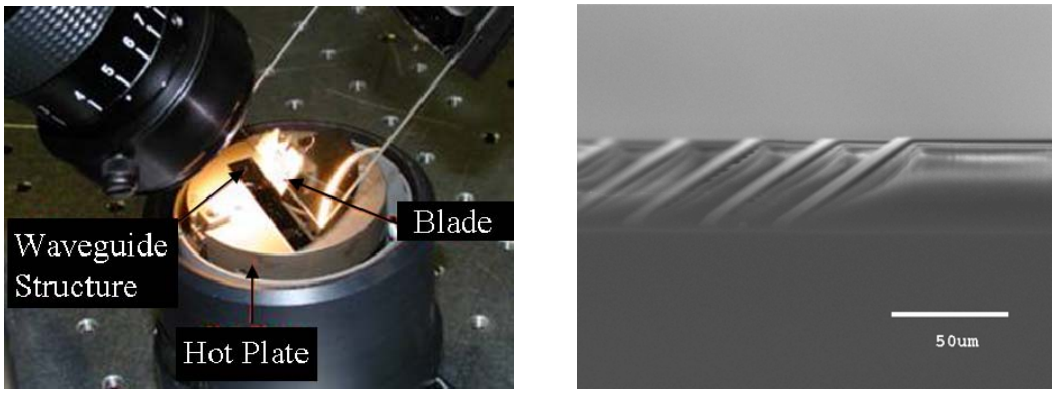


Figure 2-3 SEM pictures of the master waveguide structure on silicon wafer

45° micro-mirrors are adopted to couple a light from the VCSEL into the waveguide, and then into the PIN photodiode. To fabricate 45° micro-mirror couplers, both ends of the master waveguide structures are cut by a specially designed tool as shown in Fig. 2-4.



(A) (B)

Figure 2-4 Fabrication 45^{o} micro-mirror structure. (A) 45^{o} micro-mirror cutting tool, (B) SEM picture of fabricated 45^{o} micro-mirror structures

PDMS (Sylgard 184, Dow Corning) is chosen as a soft mold material. The PDMS is poured on the master waveguide structure and then cured. Surface relief waveguide patterns including 45° micro-mirror couplers are transferred from the master waveguide structure to the soft mold.

A flexible waveguide film is fabricated by soft molding process. The core material, UV-curable polymer, is poured on the soft mold and then excess core material is scraped out. The soft mold filled with the core material is covered with Topas^{TM} 6015 (cyclo-olefin-copolymer) film, as a bottom cladding layer. The core waveguide structure is transferred from the soft mold to Topas^{TM} 6015 film using a hot-pressing machine. A flexible waveguide film without the top cladding layer is exposed to UV light to cross-link the core material and then the surfaces of the 45° micro-mirrors are deposited with metal, aluminum (Al), to ensure total internal reflection. Finally, the top cladding material is spin-coated on the film.

Fabricated polymer waveguide film is interposed between conventional PCB (FR-4) substrates. As an adhesive layer between an optical layer and a PCB, the PSA (Pressure Sensitive Adhesive) film is inserted. Fig. 2-5 shows the cross sectional view of the laminated optical film layer on the PCB. After lamination process, the thickness of an optical film is 160 ~ 170 μm including core and cladding layers. PSA layer thickness is around 200 μm. After lamination processes, all physical dimensions of the optical waveguide structures are conserved.

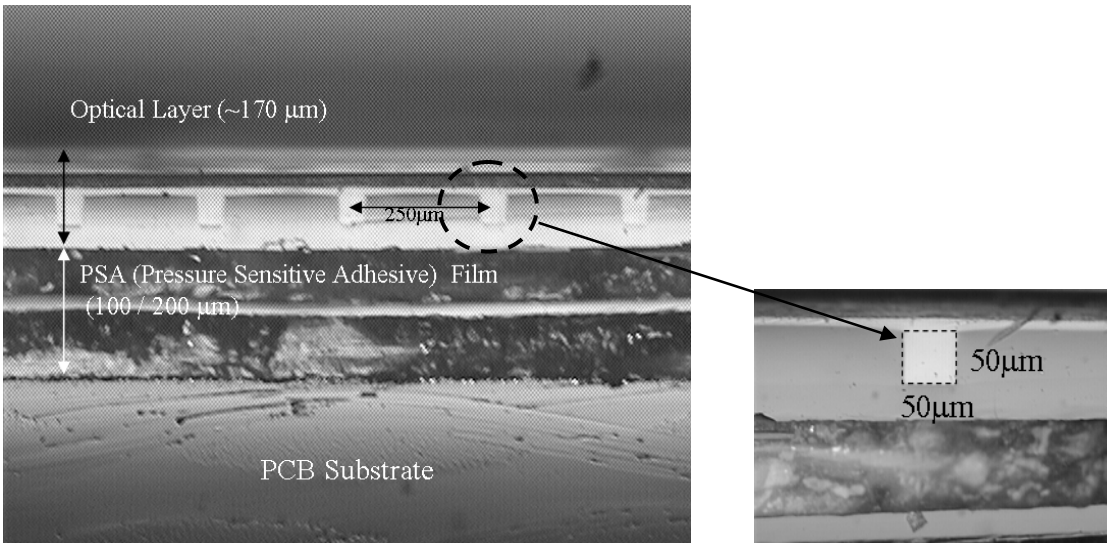
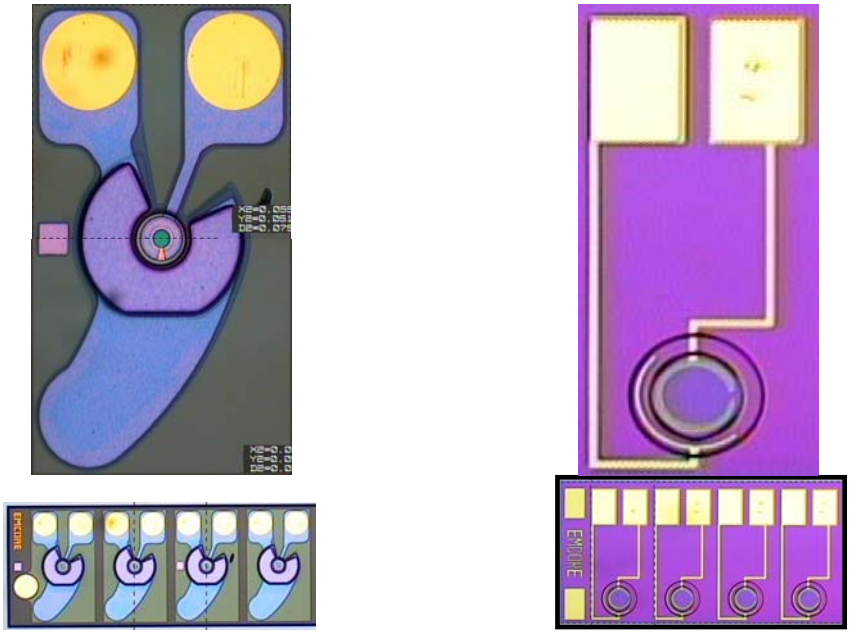


Figure 2-5 Laminated 12-channel polymer waveguide film on the PCB substrate by PSA (pressure sensitive adhesive) film

2.3. Integration of 12-channels VCSEL & PIN Photodiode Arrays on the Optical Waveguide Film

In this study, an 850 nm, 12-channel GaAs VCSEL array and a PIN photodiode array are used as transmitter and receiver optoelectronic devices. Fig. 2-6 shows an individual VCSEL and PIN photodiode. The aperture sizes (diameter) of VCSEL and PIN photodiode are 15 μm and 80 μm, respectively. Each device pitch is 250 μm in a 12-channel array structure.



(A) VCSEL array (B) PIN photodiode array

Figure 2-6 850 nm wavelength, 12-channel (A) VCSEL array and (B) PIN photodiode array

Each VCSEL and PIN photodiode is integrated on the optical waveguide film as mentioned in the previous chapter. Using the pick-and-place tool, 12 apertures of VCSEL / PIN photodiode are precisely aligned with 12 windows of waveguide structure as shown in Fig. 2-7. The thermal-compression mode is applied to attach the device onto the polymer-based optical waveguide film. The 12-channel waveguide structure is 109 cm total length and 250 μm pitch.

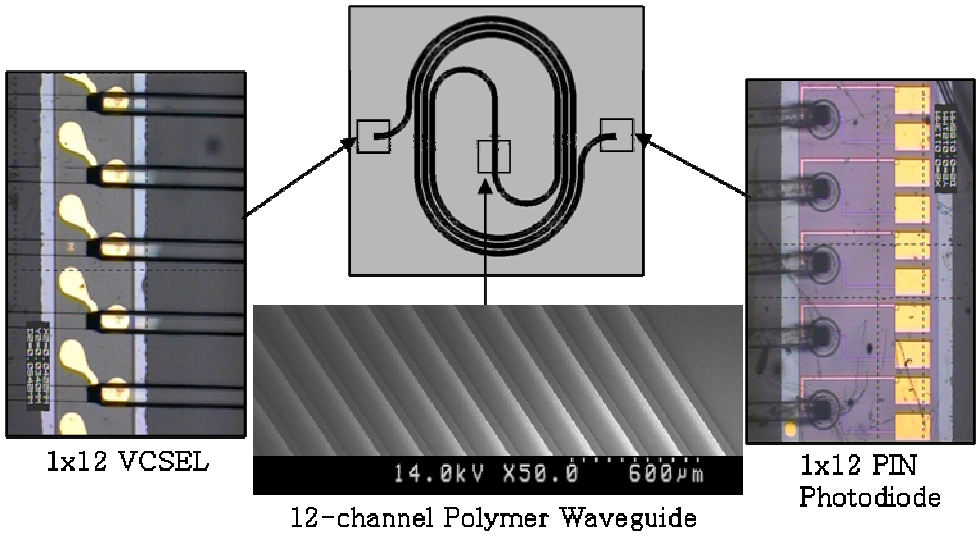


Figure 2-7 12-channel polymer waveguide film integrated with thin film VCSEL & PIN Photodiode arrays

In the fully embedded structure, electrical pads of the device are connected with outside electrical components, VCSEL drivers or PD amplifiers, through the spread transmission lines and via structures. One end of the spread transmission pattern is connected with VCSEL or PIN photodiode. The other end is connected to the outer layer through via structure. Fig. 2-8 shows the spread transmission line pattern on PCB. 12 electrical connection structures are designed for N-contact pads and P-contact pads. Between the transmission contacts and device electrical pads, gold stud bumps are located as an interconnection structure. A wire bonding machine is used to fabricate gold stud balls on the device pads. Self-coining processes are applied to terminate wire tails

from the gold stud ball. Fig. 2-9 shows the self-coined gold stud balls (dia. = 60 μm) on the electrical pads of PIN photodiode.

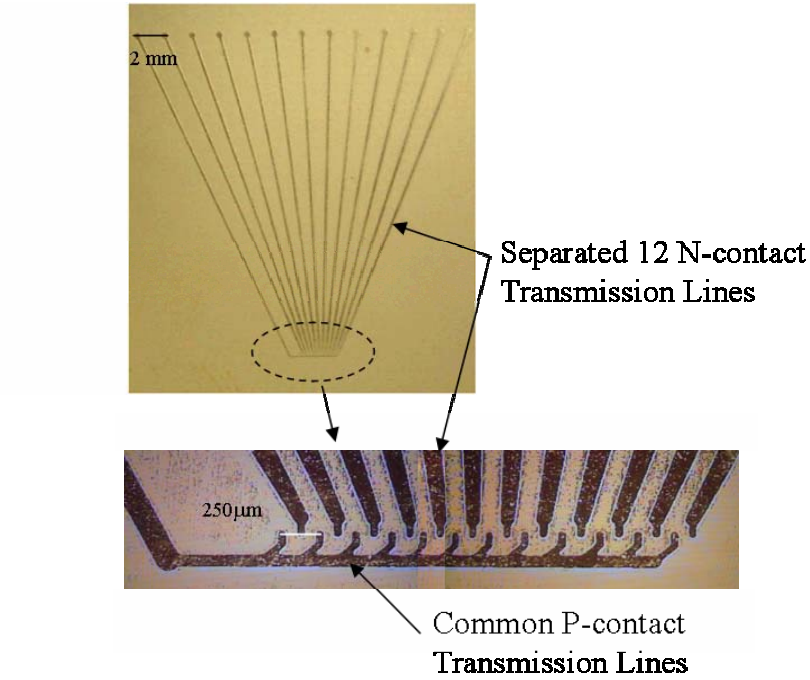


Figure 2-8 Cu-plated transmission line patterns on PC-Board and magnified view of device connection pads

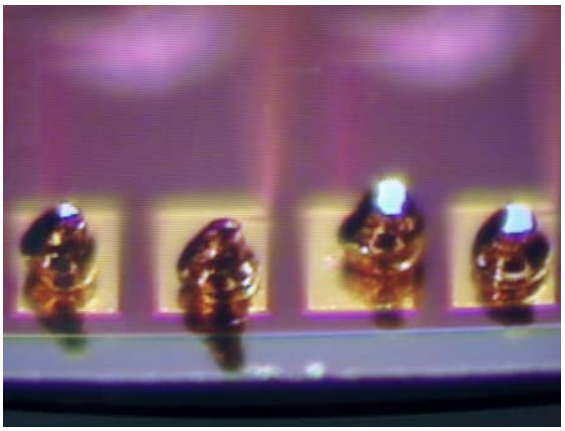


Figure 2-9 Self-coined Au-stud bumps on the electrical pads of PIN photodiode array

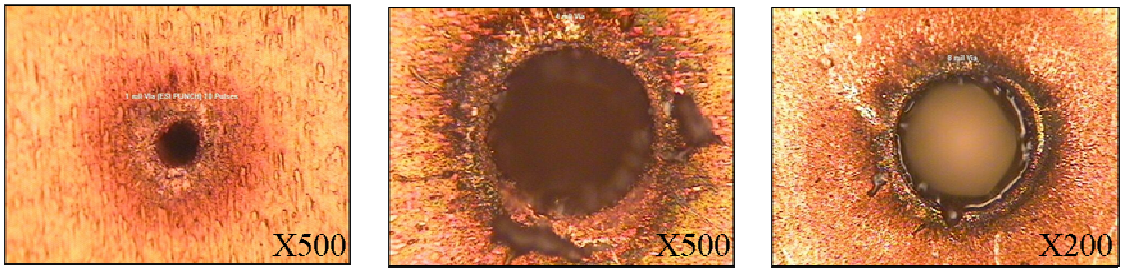


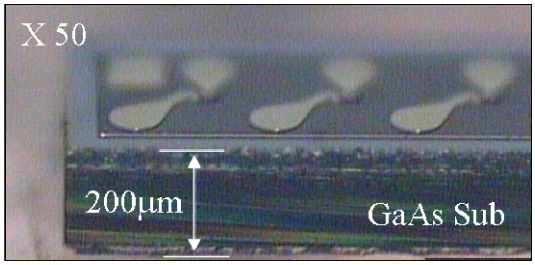
Figure 2-10 Fabricated micro-via hole on TOPAS film by CO_2 laser drill processes (SANMINA-SCI)

Micro-via holes are fabricated on TOPAS film by CO_2 laser drill processes. 1 mil (25 μm), 4 mil (100 μm), 8 mil (200 μm) diameter via holes are shown in Fig. 2-10. After via drilling on TOPAS film, the inside of the via hole is filled with Cu.

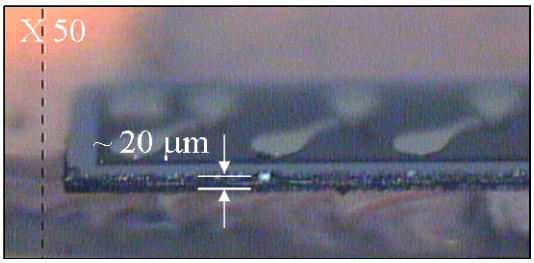
2.4. Electrical/Optical Characterizations of Substrate Thinned VCSEL and PIN Photodiode

12-channel, 850 nm VCSEL arrays (2.5 Gbps and 10 Gbps) and a PIN photodiode array are used as I/O sources on a flexible polymeric waveguide film. The initial GaAs substrate, 200 μm thickness, of VCSEL is reduced for managing the thermal resistance of

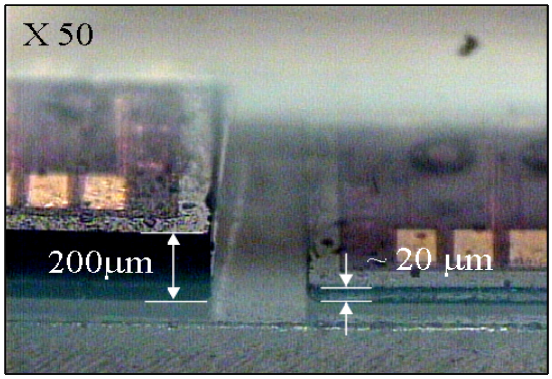
VCSEL and the fully embedded structure [28][29]. More detailed research results about thermal characteristics of thin film VCSEL are presented in chapter 4.



(A) 200 μm thick VCSEL array



(B) 20 μm thick VCSEL array



(C) Substrate thinned PIN-Photodiode

Figure 2-11 Substrate thinned VCSEL and PIN photodiode arrays

Substrate thinning processes are followed by mechanical lapping and chemical wet etching. Both VCSEL and PIN photodiode are fabricated on GaAs substrate as shown in Fig. 2-11. The initial thickness of GaAs substrate is reduced up to 80~100 μm

by a mechanical lapping and polishing process. After that, the final thickness of VCSEL (or photodiode) is controlled by wet chemical etching processes [38].

Fig. 2-12 shows a schematic diagram of measurement setup for optical properties. Electrical contact is made with micro-probes linked to a pulse pattern generator (HP-83592C). The pulse pattern generator provides the modulation by generating a 2^{23}-1 pseudorandom bit sequence (PRBS) non return-to-zero (NRZ) pattern at 10 Gbps. The emitted light is collected by a multi-mode fiber (MMF, $\varphi = 62.5$ μm) and detected by a 21 GHz bandwidth photo-receiver (Newport, D-15).

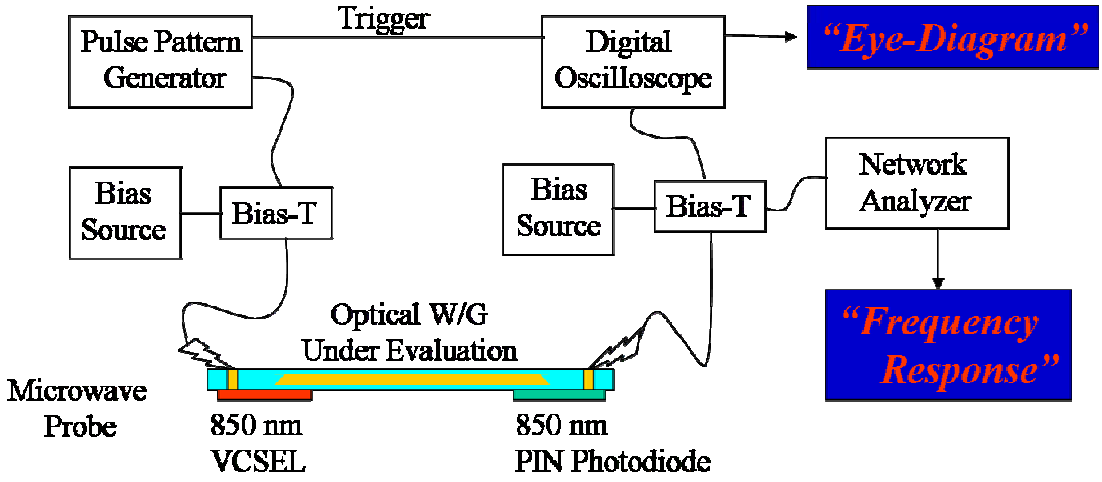


Figure 2-12 Schematic diagram of speed measurement setup

The CW L-I-V characteristics of 200 μm and 20 μm thick VCSEL are shown in Figure 2-13. Measured threshold current and slope efficiency are 0.7 mA and 0.55

mW/mA, respectively. Electrical characteristics of the substrate thinned VCSEL are the same as those of the original thick VCSEL.

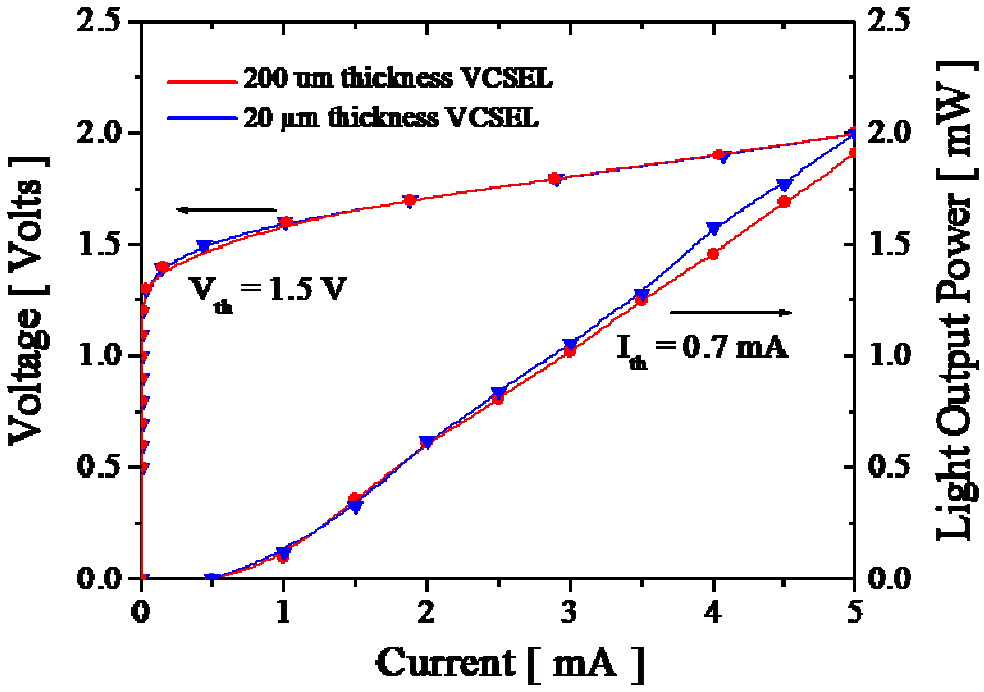


Figure 2-13 L-I-V characteristics of 200 μm and 20 μm thick VCSEL

Figure 2-14 shows a 10 Gbps eye-diagram of 20 μm thick VCSEL measured by a digital communication analyzer (HP-83480A). 2.0 V / 5.0 mA bias condition is used to operate VCSEL and 10 GHz frequency (NRZ mode, PRBS = 2^{31}-1) is applied simultaneously using bias tee. Measured 10 Gbps eye-diagram shows reasonable opening. Measured Jitter RMS and Q-factor values are 4.6 ps and 5.18, respectively.

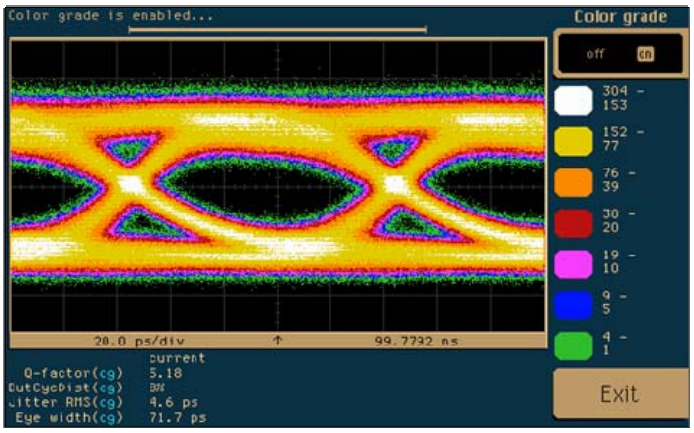


Figure 2-14 Eye-diagram of 20 μm thickness VCSEL at 10 Gbps

Measured frequency response of 20 μm thick VCSEL as a function of bias conditions, 1.0 mA ~ 5.5 mA, are shown in Fig. 2-15. 3-dB bandwidth of 20 μm thick VCSEL is extended up to 9 ~ 10 Gbps at 5.0 mA ~ 5.5 mA bias conditions.

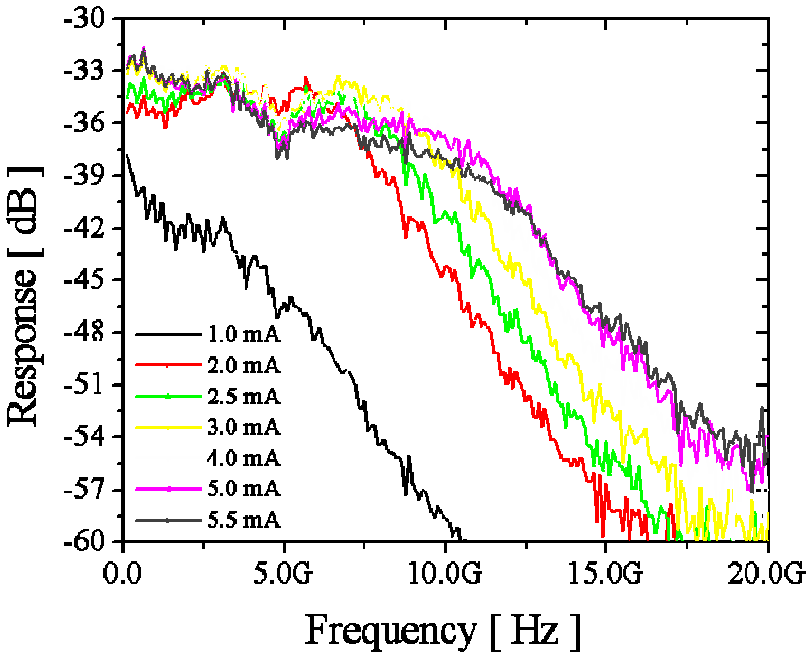


Figure 2-15 Measured frequency response as a function of VCSEL bias conditions

Measured Q-factor and Jitter RMS value variations as a function of applied frequency are shown in Fig. 2-16. With an intermediated parameter, Q-factor, the relationship of BER (Bit-Error-Rate) is given by [39]

$$BER(Q) \cong \left(\frac{1}{\sqrt{2\pi}}\right) \cdot \left(\frac{\exp\left(-Q^2/2\right)}{Q}\right) \tag{1}$$

As shown in Fig. 2-16, at 9 ~ 10 GHz frequency conditions, calculated BER of 20 μm thick VCSEL is in the range of 10^{-7} ~ 10^{-8}. Measured electrical and optical properties of substrate thinned 20 μm thick VCSEL verify that the substrate thinning process does not affect initial VCSEL characteristics.

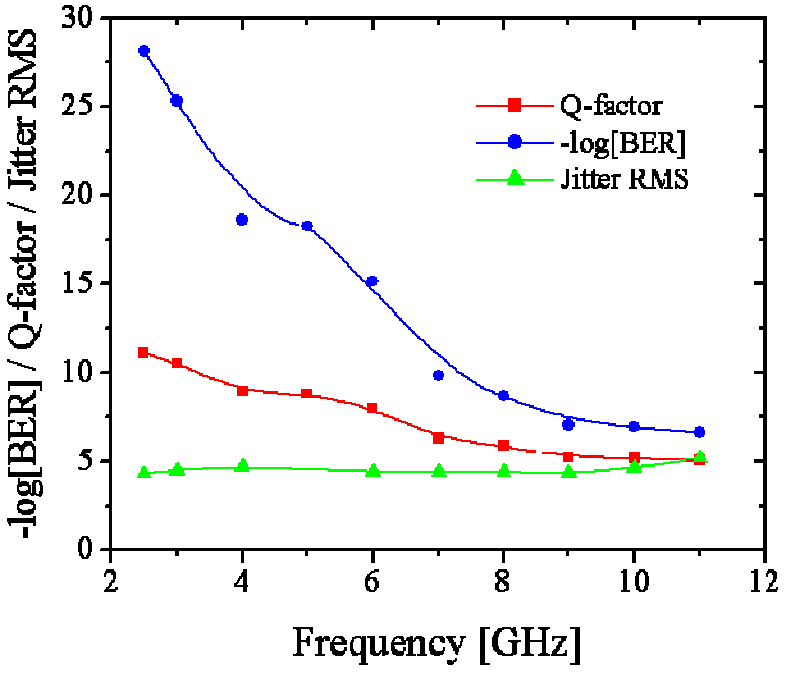


Figure 2-16 Measured Q-factor, Jitter RMS and Calculated BER as a function of applied frequency. [bias condition of VCSEL = 2V / 5 mA]

I-V characteristics of 200 μm and 20 μm thick PIN photodiode are shown in Figure 2-17. Measured dark current and photo current are in the range of 0.68 ~ 0.71 nA and 0.25 ~ 0.41 μA, respectively. Electrical characteristics of the substrate thinned PIN photodiode are the same as those of the original PIN photodiode.

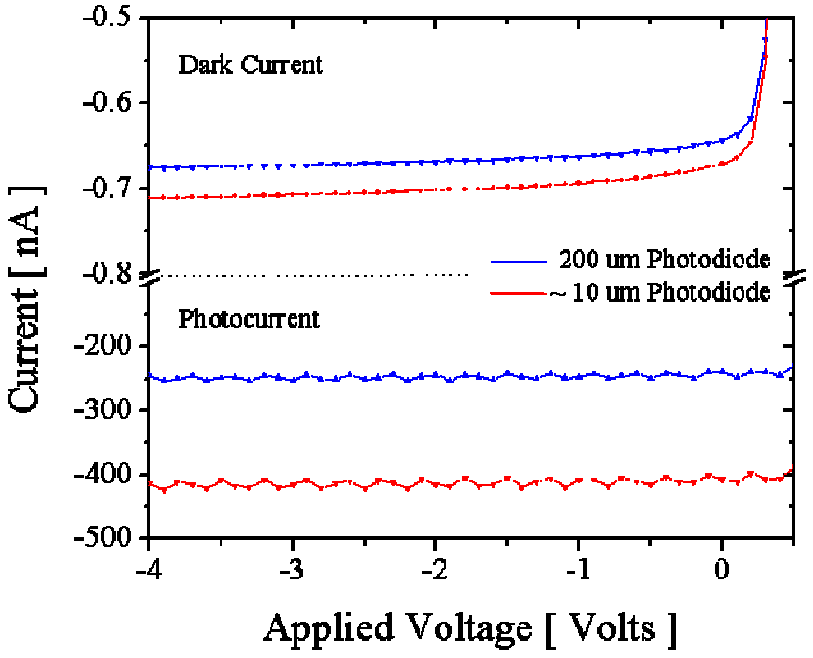


Figure 2-17 I-V characteristics of 200 μm and 20 μm thick PIN photodiode

Figure 2-18 shows a 5 Gbps eye-diagram of 20 μm thick PIN photodiode measured by a digital communication analyzer (HP-83480A). 10 Gbps VCSEL is used as an optical signal source. 2.0 V reverse bias condition is used to operate PIN photodiode and ~ 5 GHz frequency (NRZ mode, PRBS = 2^{31}-1) optical signal is coupled by multi mode fiber (dia. = 62.5 μm). Measured 5 Gbps eye-diagram shows reasonable opening.

Measured Jitter RMS and Q-factor values are 9.5 ps and 6.48, respectively.

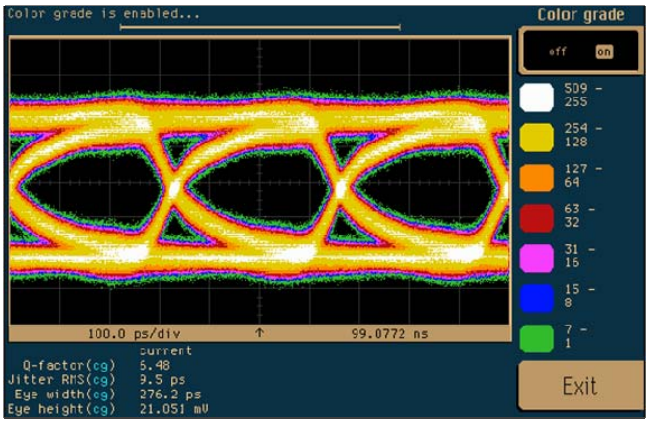


Figure 2-18 Eye-diagram of 20 μm thickness PIN photodiode at 5 Gbps

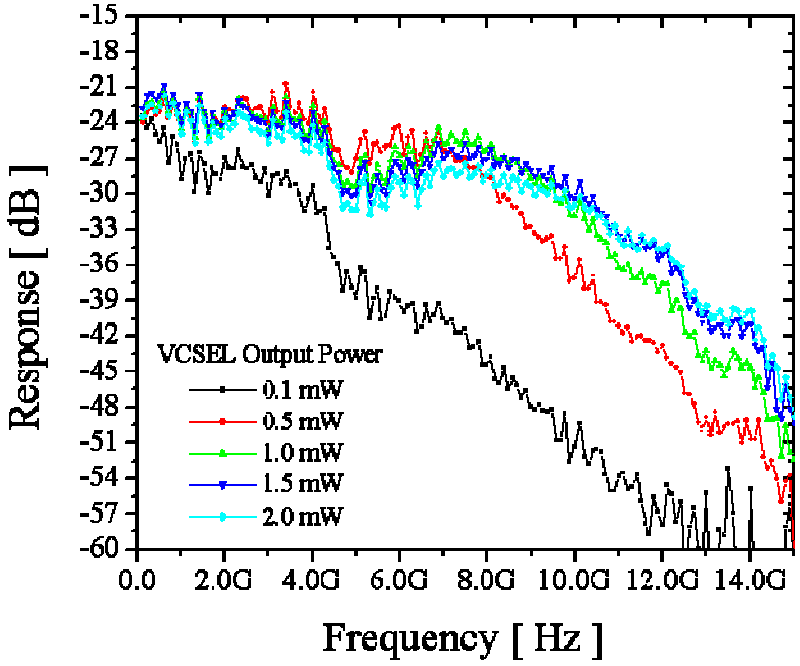


Figure 2-19 Measured frequency response variation as a function of VCSEL output power conditions

Measured frequency response of 20 μm thick PIN photodiode as a function of coupled VCSEL output power conditions, 0.1 mW ~ 2.0 mW, are shown in Fig. 2-19. 3-dB bandwidth of 20 μm thick PIN photodiode is extended up to 3 ~ 4 Gbps at 1.5 ~ 2.0 mW coupled VCSEL power conditions.

20 μm thick thin film VCSEL and PIN photodiode are coupled with 100 cm perfluorinate polymer guide. Fig. 2-20 shows measured 2.5 Gbps eye-diagram with clear opening. Measured Q-factor and Jitter RMS are 8.79 and 24.2 ps, respectively. 3dB frequency bandwidth is also extended up to 2.5 GHz at 2 mW VCSEL output beam conditions.

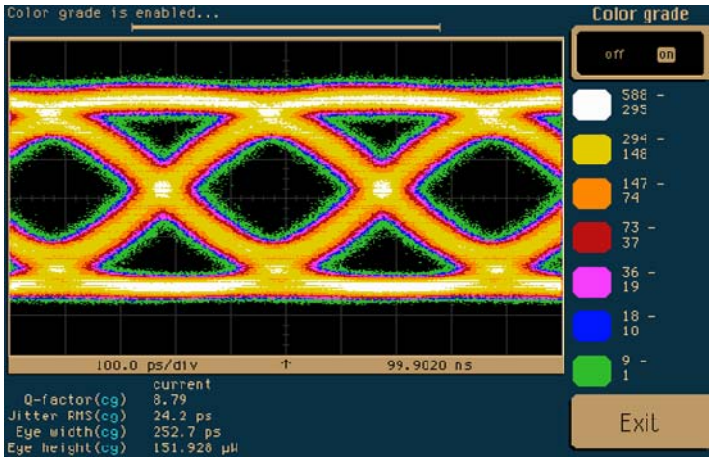


Figure 2-20 Eye-diagram of Perfluorinate polymer guide coupled with 20 μm thickness VCSEL and PIN photodiode at 2.5 Gbps

2.5. Summary

A thin flexible optical waveguide film which has a 50 x 50 mm^2 polymer waveguide array is made by the Soft-Mold process. Propagation loss of polymer waveguides is 0.1~0.6 dB/cm at 850nm. 45° TIR micro mirrors are employed to provide surface normal coupling. Electrical and optical properties of substrate removed VCSEL and PIN photodiode are characterized and integrated on a thin flexible optical waveguide film. Micro-Via formation and Optical PCB lamination processes are performed by SANMINA-SCI.

Chapter 3: Calculated Coupling Efficiencies of Spherical Micro-Mirrors for the Fully Embedded Waveguide Structure

A 45^o micro-mirror coupler is one of the critical components in an optical interconnection system, especially in planarized lightwave circuits (PLCs). In the case of the board level optical interconnection system, an optical signal beam of VCSEL is coupled into a polymer waveguide by a 45^o micro-mirror coupler which reflects the beam at a right angle. Due to the concerns about thermal management and crosstalk, a higher coupling efficiency between the waveguide and the VCSEL is required to enable the lower power operation of the VCSEL. Recently most of published results applied 45^o waveguide mirrors in their optical interconnection system to couple optical signal from VCSEL to waveguide and then from waveguide to PIN photodiode [40][41][42].

Chapter III introduces the spherical shape waveguide mirror couplers for the fully embedded board level optical interconnection system. One of the major advantages of the spherical mirror is that the divergence angle of a reflected Gaussian beam from a mirror surface can be controlled by changing the mirror radius. The variations of the coupling efficiency are calculated as a function of the radius of the spherical mirrors. A polymer waveguide array with spherical mirror couplers is fabricated using a hard glass-mold process.

3.1. Theory and Simulation Models for Spherical Mirrors

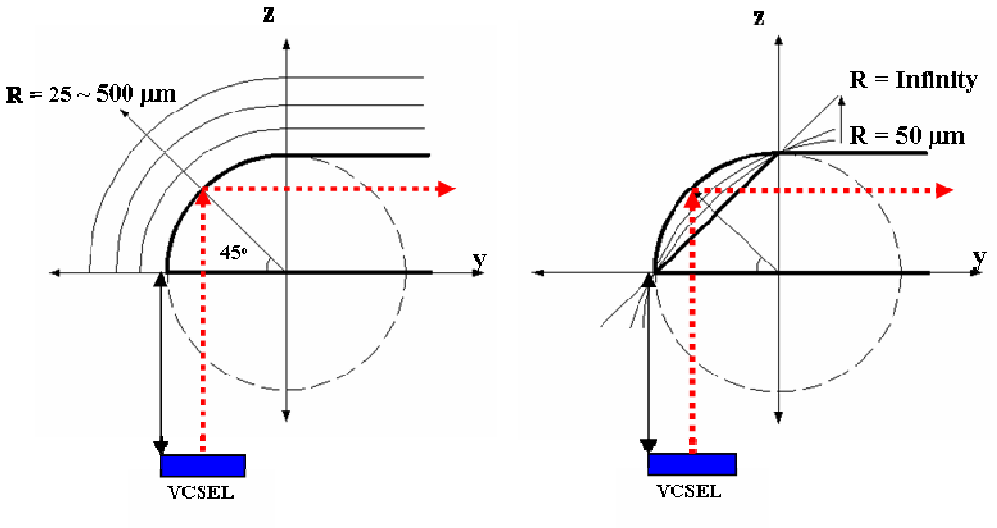
Real spatial distribution of VCSEL beams in multimode operation is not the same as an ideal single mode Gaussian profile. However we can consider it as a Gaussian

profile by ignoring the small error. Another assumption for reflected beams is the total internal reflection (TIR); Reflected beams within acceptance angle, or critical angle, of the waveguide are totally coupled into the waveguide [43].

The degree of deviation can be conveniently quantified by a quality factor M^2 called the "M-squared factor" or the "time diffraction limit number". This factor has been defined such that $M^2 = 1$ for an ideal single mode Gaussian beam. Real multimode VCSEL beams have factors greater than one. We can simply calculate the M-squared factor using different divergence angles between an ideal beam (θ_0) and the real beam (Φ_0). An ideal Gaussian beam divergence angle (θ_0) can be calculated from beam wavelength (λ) and the beam waist (ω_0) of VCSEL [44].

$$\Phi_0 = M\theta_0, \quad \theta_0 = \frac{\lambda}{\pi\omega_0} \tag{3-1}$$

This factor can be used to compare real VCSEL beams to a single mode beam and allow the use of the properties and equations which have been developed for Gaussian beams. To calculate coupling efficiency, we need to know the VCSEL beam intensity distribution and propagation angle at spherical mirror surface. Fig. 3-1 illustrates a waveguide with a spherical mirror. There are two simulation models for spherical mirror structure. In Model-1, shown in fig. 3-1 (A), spherical mirror radii are changed at fixed waveguide dimension conditions. As mirror radius increases, the mirror surface becomes flattened but the waveguide dimensions are not changed. In Model-2 shown in figure 3-1 (B), a waveguide radius increases simultaneously as the spherical mirror radius increases.



(A) Model-1 (B) Model-2

Figure 3-1 Simulation models for spherical mirror coupler. (A) Model-1; spherical mirror radius is changing at fixed waveguide dimensions, a half cylindrical shape waveguide with 100 μm diameter (B) Model-2; spherical mirror radius is changing simultaneously with waveguide dimensions

The VCSEL is attached on a flexible transparent film so that the VCSEL beam travels through the transparent film and is reflected at mirror surface. The flexible transparent film is optically isotropic. There are about 40 supporting modes in the 50 μm square waveguide. For exact calculation we have to consider all modes but the number of mode is quite large. The VCSEL beam can be treated as geometrical optics (Ray optics). To calculate coupling efficiency, we need to know the intensity distribution and propagation angle at spherical mirror facet. Propagation angle at mirror surface $\theta(r,z)$

can be calculated from the radius of curvature of wavefront ***R(z)*** and distance from the center ***r.***

$$\theta(r,z) = \sin^{-1}(\frac{r}{R(z)}) \tag{3-2}$$

The radius of curvature ***R*** at any ***z*** of the wave-front is given by equation

$$R(z) = z\left(1 + (\frac{z_0}{z})^2\right) \quad , \quad z_0 = \frac{\pi\omega^2{}_0 n}{\lambda} \quad , \quad \omega(z) = M\omega_0\sqrt{1 + \left(\frac{z}{z_0}\right)^2} \tag{3-3}$$

where, λ is wavelength, ω_0 is the beam waist at VCSEL surface and $\omega(z)$ is the beam width at ***z***. The optical intensity is a function of the axial and redial distances z and $r = \sqrt{x^2 + y^2}$. The total optical power carried by the beam is the integral of the optical intensity over a transverse plane. The electric field distribution ***E(r,z)*** of a Gaussian beam in a homogeneous medium is given by

$$E(\mathrm{r},\mathrm{z}) = E_0 \frac{\omega_0}{\omega(z)} e^{\left\{-i[kz-\delta(z)]-(r^2)[\frac{1}{\omega^2(z)}-\frac{ik}{2R(z)}]\right\}} \tag{3-4}$$

and the intensity distribution of the Gaussian beam is

$$I(r,z) = \left|E(r,z)\right|^2 = E_0\left\{\frac{\omega_0}{\omega(z)}\right\}^2 e^{\left(-2(r^2)\frac{1}{\omega^2(z)}\right)} \tag{3-5}$$

Therefore, the coupling efficiency, η can be calculated by

$$\eta = \frac{\int_{-r_c}^{r_c} |E(r,z)|^2 \, dr}{\int_0^{\infty} |E(r,0)|^2 \, dr} = \left(\frac{\omega_0}{\omega(z)} \right)^2 \int_{-r_c}^{r_c} |E(r,z)|^2 \, dr \qquad (3\text{-}6)$$

where, $\boldsymbol{r_c}$ is the maximum radius at the mirror facet which corresponds to the acceptance angle of the waveguide.

The coupling efficiencies of spherical mirrors are calculated at variable mirror radii, different Δn (refractive index difference between core and cladding) and substrate thickness (bottom cladding) conditions.

3.1.1. Mirror Radius Changing with Fixed Waveguide Dimensions (Model-1)

The coupling efficiencies for Model-1 are calculated using the Matlab software. In Model-1, we assumed a half cylinder shape waveguide structure with a 50 μm radius. The spherical mirror radius and the thickness of the optical bottom layer are changed as calculation parameters.

Calculated coupling efficiencies of the spherical mirror, Model-1, was shown in Fig. 3-2. Due to the focus effect of the spherical mirror, the radius of curvature of the wavefront ***R(z)*** is reduced. Therefore, more incident beams can be coupled into a waveguide within a critical range of mirror radii. This result shows that the spherical mirror has a maximum (or optimum) coupling efficiency within the critical range of mirror radii from 185 μm to 1000 μm. As a mirror radius increases above the critical range, the coupling efficiency is reduced and then finally saturated. The saturated

coupling efficiency of the spherical mirror has the same coupling efficiency of a 45° flat mirror.

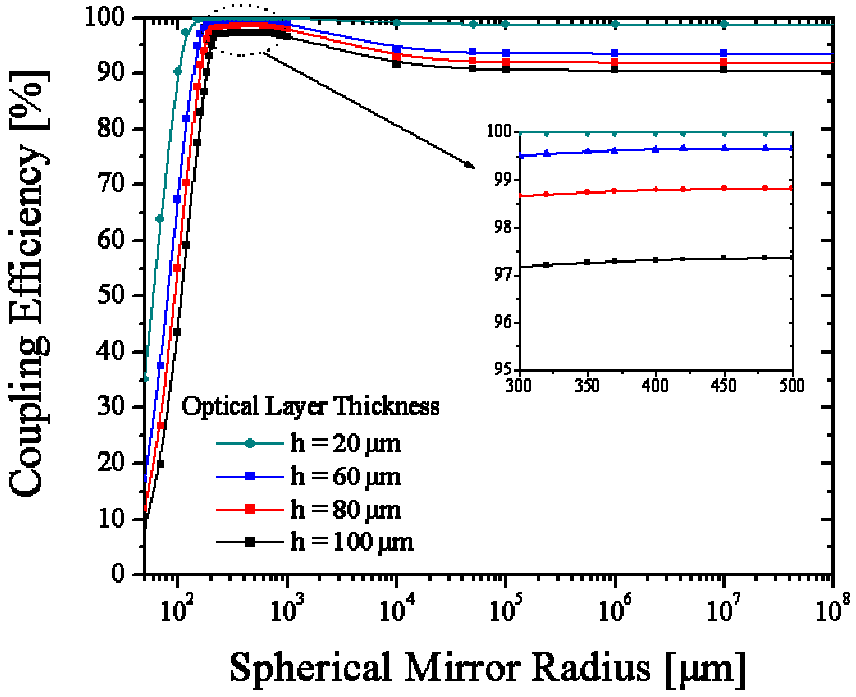


Figure 3-2 Calculated coupling efficiencies of Model-1 spherical mirror as variable mirror radius and thickness of optical bottom layer (h). [Δn = 0.02]

In the case of the 100 μm thickness of optical bottom layer condition, the calculated coupling efficiency of a 45° flat mirror is 90.5%. The maximum (or optimum) coupling efficiency of a spherical mirror is 97.63% at a 480 μm mirror radius. The calculated coupling efficiency difference between a 45° flat mirror and a spherical mirror with a 480 μm mirror radius is about 7 %. In the range of mirror radii from 185 μm to

1000 μm, the coupling efficiency of the spherical mirror is better than that of the 45° flat mirror.

As the thickness of the optical bottom layer is reduced from 100 μm to 20 μm, the maximum and the saturated coupling efficiency are increased up to 100 %. However, the difference between the coupling efficiency of a 45° flat mirror and a spherical mirror is almost same. In the case of the 20 μm thickness of optical bottom layer condition, the coupling efficiency difference between a 45° flat mirror and a spherical mirror is 1.2 %.

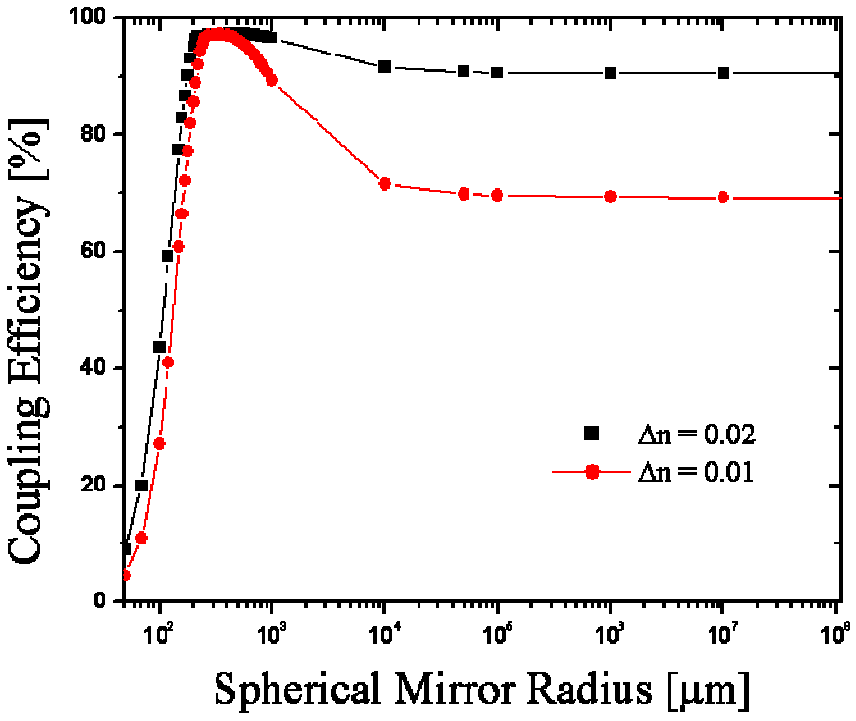


Figure 3-3 Calculated coupling efficiencies of spherical mirror as variable mirror radius and different Δn (refractive index difference between core and cladding). [thickness of optical bottom layer (h) = 100 μm]

As the refractive index difference between core and cladding decreases, the coupling efficiency difference between a 45^o flat mirror and a spherical mirror increases. In the case of $\Delta n = 0.01$, the calculated coupling efficiency difference between a 45^o flat mirror and an optimum spherical mirror is 27.9 %.

3.1.2. Mirror Radius Changing with Waveguide Dimension (Model-2)

In Model-2, we assumed that the dimensions of a half cylinder shape waveguide are changed simultaneously with the spherical mirror radius. The spherical mirror radius and the thickness of the optical bottom layer are changed as calculation parameters. As a spherical mirror radius increases with the waveguide diameter, the coupling efficiency is increases. In fig. 3-4, the calculated coupling efficiencies with different optical layer thicknesses (0.02 μm and 0.01 μm) at a 500 μm mirror radius are 79.3 % and 93.1 % respectively. Figure 3-5 shows the intensity distributions of a VCSEL beam at spherical mirror surface for a 10 μm thick optical layer, radius of mirror, and waveguide of 500 μm.

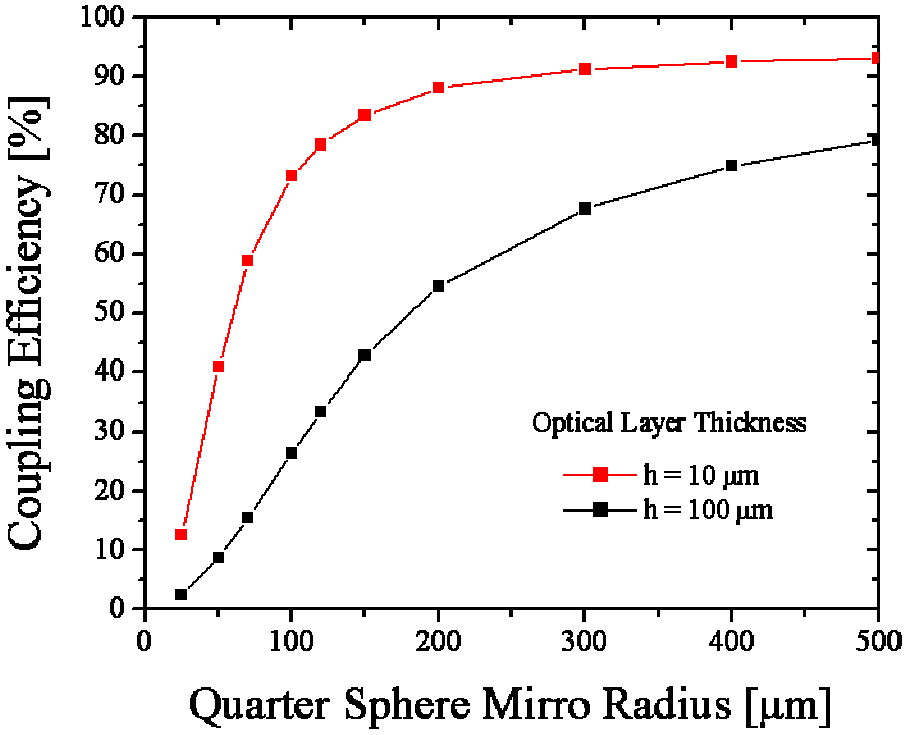


Figure 3-4 Calculated coupling efficiencies of Model-2 spherical mirror as variable mirror radius and different thickness of optical bottom layer (h). [$\Delta n = 0.02$]

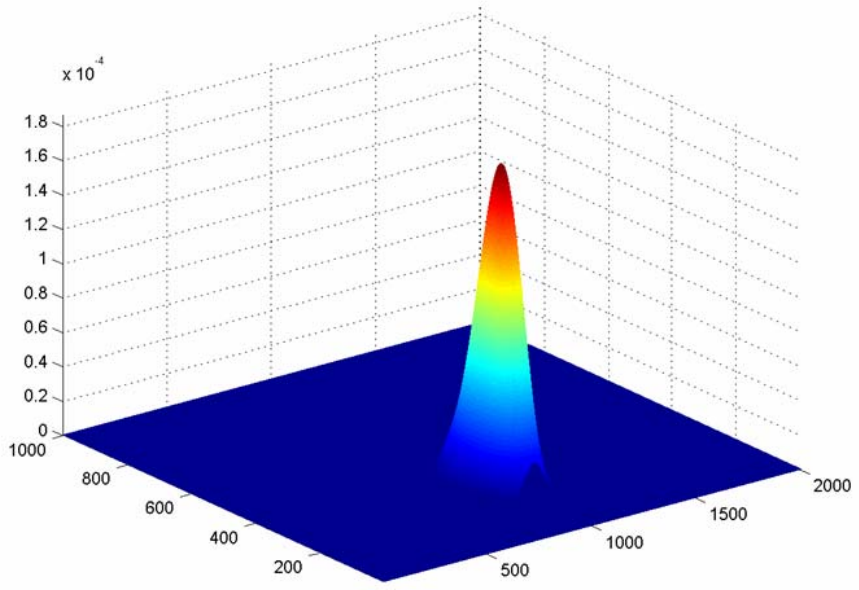


Figure 3-5 Spherical mirror coupled beam intensity distributions with 10 μm thick optical layer at 500 μm mirror radius conditions

3.2. Fabrication of a Half Cylinder Shape Waveguide with Spherical Micro-Mirror

There are various fabricating techniques to define the optical waveguide on myriads of substrates. Hot embossing and molding are indirect fabrication techniques in which the waveguide structure is transferred onto the substrate. An embossing plate or cast is first fabricated using the master waveguide pattern. Once the plate or the cast is fabricated, the rest of processes are purely replication steps. Therefore, these fabrication techniques are suitable for mass production, like the stamping of compact disks. The hard molding method was chosen in this experiment because of its dependable process and

suitability for large volume production even though only a small quantity is needed in research stage. The hard mold is generally used in various applications such as embossing, optical disk stamping, and Fresnel lens fabrication. A conventional hard mold is made of nickel alloy by electroplating. The fabrication of the hard mold has a higher cost and making a circular shape mirror structure at the end of waveguide pattern is almost impossible. For these reasons we seek alternative hard mold materials.

We use a soda-lime glass plate as a mold material, which is mainly used for the fabrication of lithography masks. Because soda-lime glass has an amorphous structure, it exhibits an isotropic etching behavior in wet chemical etching [45]. This permits the fabrication of a nearly sphere shaped mirror structure at the end of a half cylinder shape waveguide pattern.

The soda-lime glass is wet etched with hydrofluoric acid containing etchants. The etch products are soluble in water, and also in the etch solution. The etch mask preparation for the etching processes is of great importance, since the mask determines the properties of the final waveguide and mirror structures, i.e. wall roughness, radius accuracy of mirror and waveguide, etc. The Cr metal mask is deposited as an etch mask on a soda-lime glass plate.

Figure 3-6 shows the glass hard mold fabrication process for the realization of the waveguide with a nearly sphere shaped mirror in soda-lime glass plate. Common lithography processes are employed for the waveguide pattern fabrication on a Cr deposited soda-lime glass. The final waveguide dimensions, including mirror radius, are controlled by the wet etching rate. The composition of the acid solution used for the

isotropic wet etch is BOE (49%):HCl:H_2O = 1:2:16. The etching rate of this solution is 0.18 μm/min.

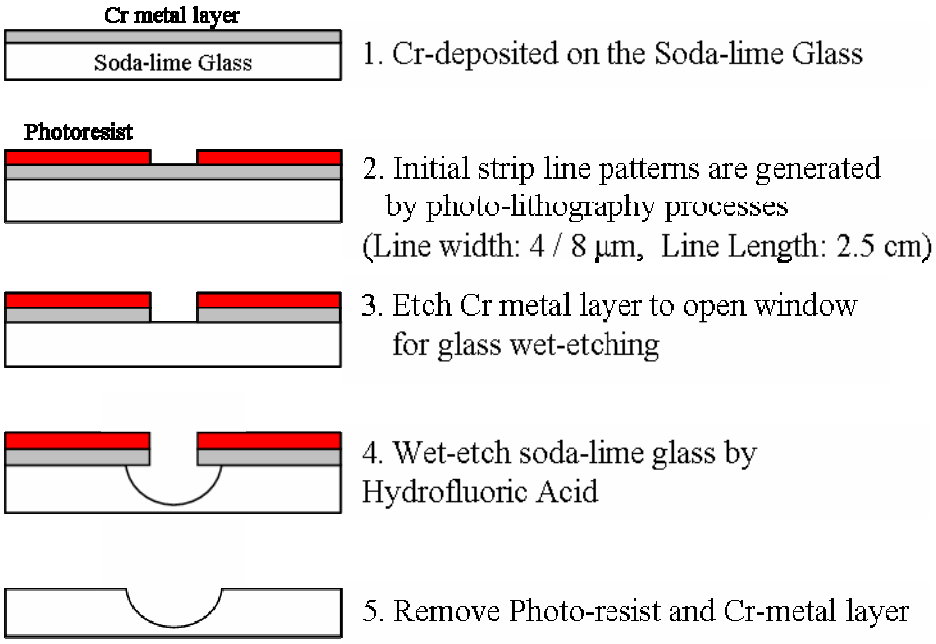


Figure 3-6 Fabrication of a half cylinder shape waveguide with sphere mirror on the glass substrate as a hard mold

Figure 3-7 displays a detail of an isotropic etched structure including dimensions of the waveguide structure and mirror circle radius. The initial opening of Cr metal is 4 μm and a soda-lime glass is wet etched around 50 μm. However, due to the interface effect between Cr metal and soda-lime glass, the etching rate of the lateral direction is slightly faster than that of the vertical direction. Cross section views in fig. 3-7 show that mirror radius and waveguide gradually increase to the lateral direction at the glass mold

surface. Fabrication of the spherical micro-mirror is experimentally restricted due to the deficiency of fundamental research results. To reduce surface roughness of etched region, high purity glass should be selected as a mold material. Also spherical micro-mirror curvature should be controllable by wet etching parameters.

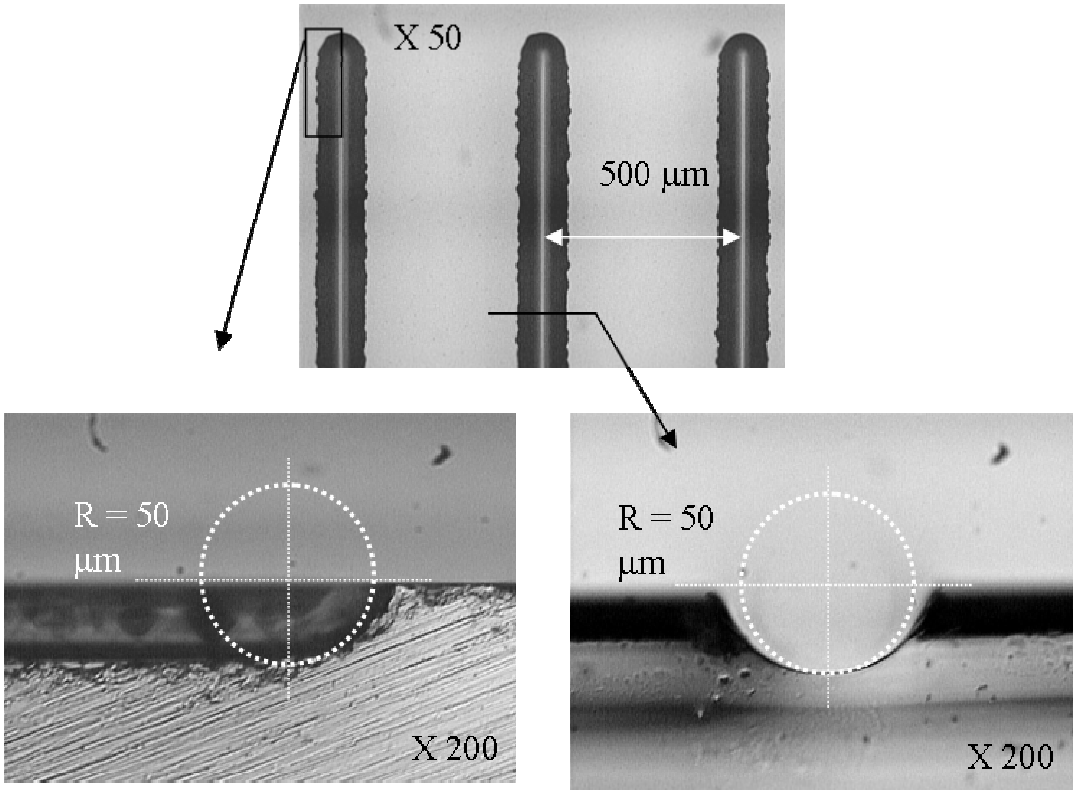


Figure 3-7 Hard glass mold with a half cylinder shape waveguide pattern and a quarter sphere shape mirror coupler

3.3. Summary

The optimum shapes of micro-mirror structures for a fully embedded optical interconnection system are studied. The coupling efficiencies as a function of radius of quarter-sphere shape micro-mirror structures are theoretically calculated. In the case of model-1, due to the focus effect of spherical mirror, more incident beam can be coupled into a waveguide. The mirror radius range between 450 μm to 470 μm shows the maximum coupling efficiency in this study. As increase a mirror radius above the critical range, the coupling efficiency is gradually reduced and then finally saturated. The saturated coupling efficiency with a mirror radius above the maximum range is the same as the coupling efficiency of 45^{o} flat mirror.

A soda-lime glass hard mold is fabricated to make a waveguide pattern with a sphere shape mirror structure. Nearly sphere shape mirror structure is fabricated by the isotropic wet-etching processes. To make a waveguide pattern with a sphere shape mirror structure, however, need more researches to precisely control the mirror radius with the different etch-mask materials.

Chapter 4: Effects of Thermal-Via Structures on Thin Film VCSELs for Guided-Wave Optical Interconnection System

4.1. Thermal Management of Thin Film VCSEL

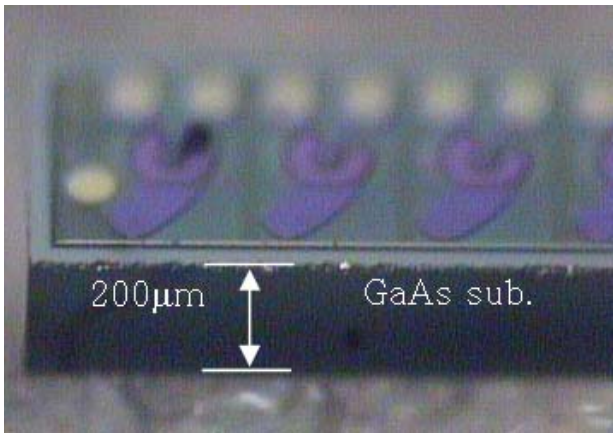
To relieve packaging difficulty, we have developed the fully embedded board-level optical interconnection system which is also depicted in chapter 3. All the optoelectronic components including VCSEL array, PIN photodiode array, TIR coupling mirror and planar polymer waveguides are integrated within the 3-D interconnection layers during the conventional PCB fabrication processes. In this architecture, however, the self-heating effect of the vertical-cavity surface-emitting laser (VCSEL) cause critical issues in the system reliability since integrated VCSEL arrays are surrounded by thermal insulators such as optical polymer films(TOPAS®) and PCB bonding materials (prepreg or pressure-sensitive-adhesive film). Because the operating lifetime of VCSEL decreases exponentially with temperature [46], the thermal management of the embedded VCSEL arrays is one of the primary concerns in the fully embedded optical interconnection system. G. Chen *et al.* [47] and Y. Liu *et al.* [48] have reported device-level investigations on the thermal characteristics of VCSEL. Also, comprehensive studies on the thermal resistance of an integrated VCSEL array on PCB were performed by Y. C. Lee *et al.* [49], R. Pu *et al.* [50] and A.V. Krishnamoorthy *et al.* [51]. Those papers presented valuable results, but the results are not applicable to our system directly because of the different integration structures.

This chapter presents theoretical and experimental studies of the thermal characteristics of the fully embedded thin film VCSEL array which determines the effective thermal via structures. The thermal resistances as a function of the substrate thickness of VCSEL are experimentally measured. 2-D finite-element analysis is performed to simulate the temperature field distribution near and across the active region inside VCSEL as a function of the substrate thickness of VCSEL and the thermal via structure. Not only the heat generation in the active region but also the joule heating (I^2R) effect in the distributed Bragg reflectors (DBRs) are considered by the thermal-electric direct coupled-field analysis.

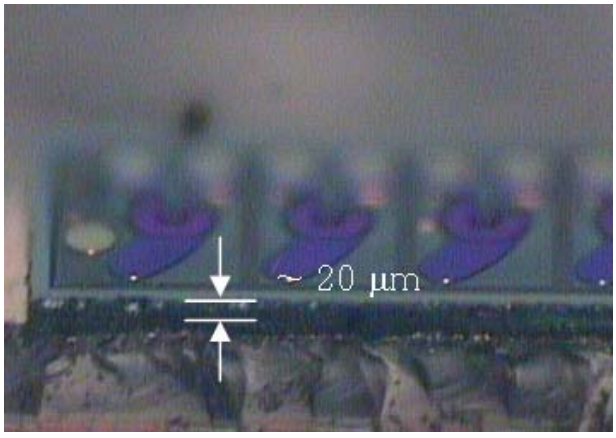
4.2. Fabrication of thin film VCSEL & measurement of thermal resistance (R_{th})

A 12-channel 850 nm oxide-confined VCSEL array with 10 Gbps each is employed as an input light source. The initial 200 μm thick GaAs substrate of VCSEL is removed not only for facilitating the fully embedded integration structure but also for managing VCSEL temperature as previously mentioned.

The initial GaAs substrate of VCSEL is reduced down to 100 μm by mechanical lapping and polishing processes. After the mechanical thinning, the thickness of VCSEL, within the range of 100 μm to 10 μm, is precisely controlled by the wet chemical etching process [52]. Fig. 4-1(A) and (B) show a part of the VCSEL array before and after the substrate thinning processes, respectively.



(A)



(B)

Figure 4-1 (A) 200 μm thick VCSEL array (before substrate thinning), (B) 20 μm thick VCSEL array (after substrate thinning)

The CW L-I characteristic variations of VCSEL as a function of temperature are shown in Fig. 4-2. At room temperature, measured threshold current and slope efficiency are 0.7 mA and 0.55 mW/mA, respectively. Fig. 4-2 shows that measured characteristic

temperature (T_o), indicating the temperature sensitivity of the threshold current, is in the range of 150 ^{o}K ~ 155 ^{o}K for the studied VCSEL.

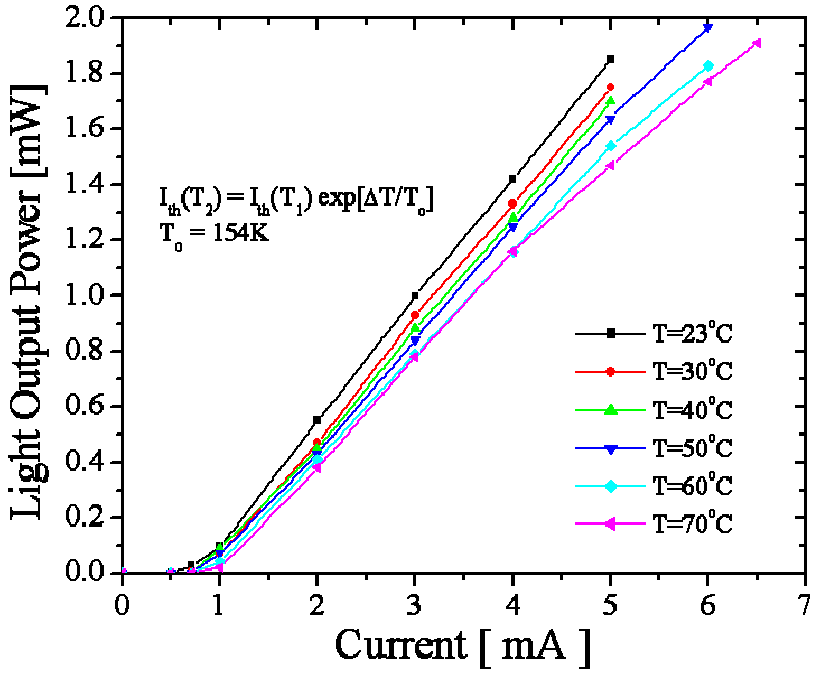


Figure 4-2 L-I characteristics of VCSEL as a function of operating temperature

Due to the self-heating effect of VCSEL, the temperature of active region rises relative to the heat sink. To achieve maximum VCSEL reliability in the fully embedded structure, it is imperative to control VCSEL temperature during operation. The ratio of temperature rise (ΔT) to the net dissipation power (ΔP_{diss}) is defined as the thermal resistance (R_{th}). The thermal resistance (R_{th}) evaluation of the VCSEL as a function of substrate thickness is performed by measuring the wavelength shift with both the

temperature ($\Delta\lambda/\Delta T$) and the net dissipated power ($\Delta\lambda/\Delta P_{diss}$). The thermal resistance is given by

$$R_{th} = \Delta T / \Delta P_{diss} = (\Delta\lambda/\Delta P_{diss}) / (\Delta T/\Delta\lambda) \quad (4\text{-}1)$$

Where, ΔT is the temperature rise in the active region, ΔP_{diss} is the change of electrical power dissipated in VCSEL and $\Delta\lambda$ is the wavelength shift. A VCSEL array is mounted on a thermoelectric cooler (TEC) to precisely control the substrate temperature at $25^{o}C \pm 1$. Measured wavelength temperature variation ($\Delta\lambda / \Delta T$) is 0.066 nm/^{o}C.

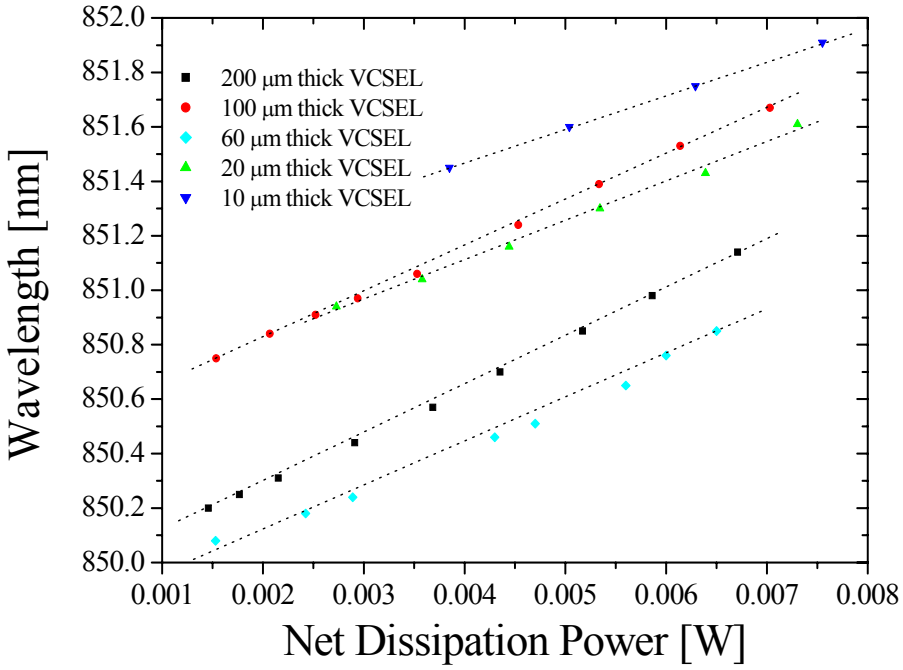


Figure 4-3 Measured wavelength shift variations as a function of net dissipated power

In Fig. 4-3, the slopes of the wavelength shift as a function of net dissipated power ($\Delta\lambda / \Delta P_{diss}$) for 200 μm, 100 μm, 60 μm, 20 μm and 10 μm thick VCSELs are 188 nm/W, 169 nm/W, 153 nm/W, 144 nm/W and 120 nm/W respectively. Experimentally measured thermal resistance values for each device are 2848 ^{o}C/W, 2560 ^{o}C/W, 2326 ^{o}C/W, 2181 ^{o}C/W and 1830 ^{o}C/W.

4.3. Numerical Modeling of Self-Heating Effect for Thin Film VCSEL

Several studies on the self-heat generation mechanisms inside VCSEL have been reported [47][48]. There are two major heat sources. One is the resistive joule heating when a current flows through the DBRs, and the other one is the non-radiative recombination of electrons and holes in the active region. To simulate the inside VCSEL temperature rise, the heat source distributions inside VCSEL have to be determined. In this chapter, a 2-D thermal-electric direct coupled-field analysis module in ANSYS software is used to calculate the temperature distribution due to the joule heating in the DBRs and the non-radiative recombination in the active region. In this simulation, we assumed that VCSEL has azimuthal symmetry. To consider interface and boundary scattering effects of phonons and electrons, anisotropic material properties are used in DBR region. Table I lists the electrical and thermal properties used in this simulation.

Table 4-1 Materials properties & physical dimensions used in simulation

	Thermal conductivity (W/μm-K)		Electrical conductivity (Ω^{-1}-μm^{-1})		Thick (μm)
p-DBR	k_r / k_z	1.2 X 10^{-5}/ 1.0 X 10^{-5}	σ_r / σ_z	2.016 X 10^{-3}/ 1.5 X 10^{-5}	3.30
n-DBR	k_r / k_z	1.2 X 10^{-5}/ 1.0 X 10^{-5}	σ_r / σ_z	4.03 X 10^{-2} / 2.85 X 10^{-4}	3.497
Substrate	$k_r = k_z$	4.5 X 10^{-5}	$\sigma_r = \sigma_z$	3.3 X 10^{-2}	10~200
Au	$k_r = k_z$	3.1 X 10^{-4}	$\sigma_r = \sigma_z$	45.4	0.2
Copper	$k_r = k_z$	3.86 X 10^{-4}	$\sigma_r = \sigma_z$	58.8	0~200
Polymer	$k_r = k_z$	2.0 X 10^{-7}	$\sigma_r = \sigma_z$	10^{-18}	30~100

The thermal-electric simulation is limited to the steady-state analysis. First, the electric field analysis is performed to calculate the current density distributions inside the VCSEL near the active region. Then, the thermal analysis is conducted to calculate the joule heating and the temperature distributions inside VCSEL. The local heat generation rate due to the joule heating is calculated by

$$q = \sigma_z \left(\frac{\partial V}{\partial z} \right)^2 + \sigma_r \left(\frac{\partial V}{\partial r} \right)^2 \tag{4-2}$$

where σ_z and σ_r are the electrical conductivity in the z-axial and the radial directions, respectively [47]. A 2-volt potential drop boundary condition, equivalent to our experimental work, is used for the electric field analysis. The steady-state heat conduction equation for the axial symmetric structure is governed by

$$k_z \frac{\partial^2 T}{\partial z^2} + k_r \frac{\partial^2 T}{\partial r^2} + q(z,r) = 0 \tag{4-3}$$

where, q is the local heat generation rate. k_z and k_r are the thermal conductivity along the z-axial and the radial directions, respectively [53].

Fig. 4-4 shows a mesh generated 2-D modeling structure of VCSEL near the active region. Both the Si-doped n-type DBR and the C-doped p-type DBR consist of stacks of quarter-wavelength layers of GaAs and $Al_{0.9}Ga_{0.1}As$. The current aperture and the active region are located between the two reflectors. Symmetric and adiabatic boundary conditions are applied on the side wall and the top surface of the modeling structure. The boundary condition for the bottom surface of Cu plate is 25°C.

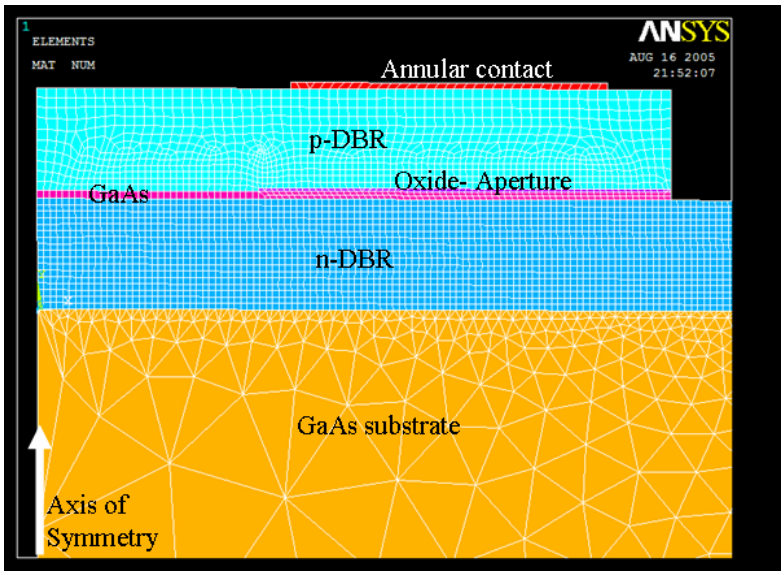


Figure 4-4 Mesh generated 2-D modeling structure of VCSEL near the active region

The radial distributions of temperature rise and heat generation density near the active region are shown in Fig 4-5. According to the electrical potential distribution inside VCSEL, most of the voltage drop occurs across the p-type DBR.

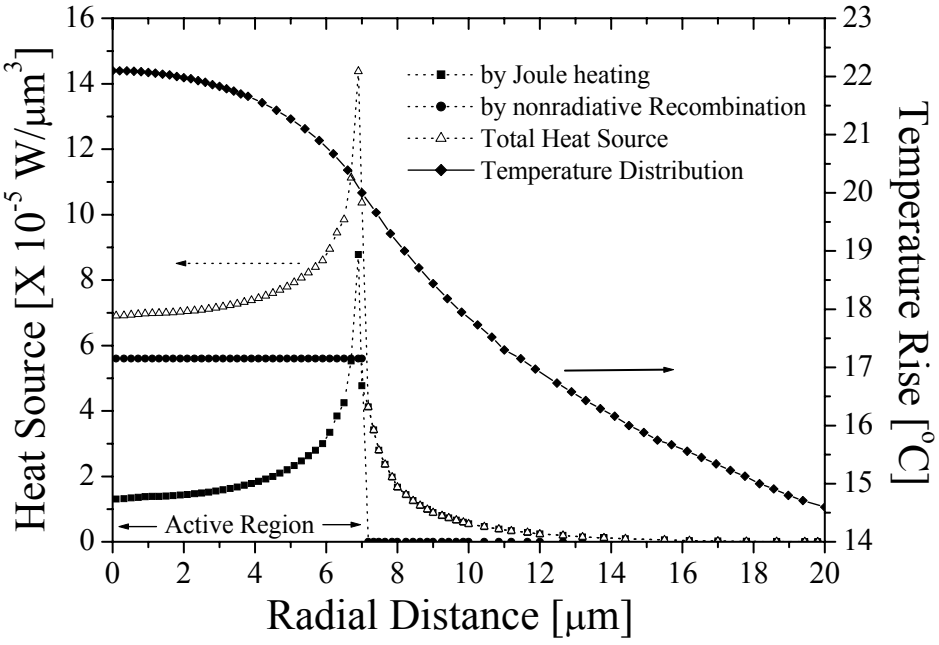


Figure 4-5 Heat source and temperature distribution of 200 μm thick VCSEL near the active region (5 mA/2 V bias condition)

As shown in Fig. 4-6, an abrupt voltage drop near the edge of the active region indicates a strong current concentration when a great portion of the current converges into the active region. This current concentration gives rise to a heat source spike at the edge of the active region as shown in Fig. 4-5. However, this spike shaped heat source distribution does not cause a local temperature peak distribution. The temperature distribution peaks along the optical axis. These observations are consistent with the results of G. Chen's results [47].

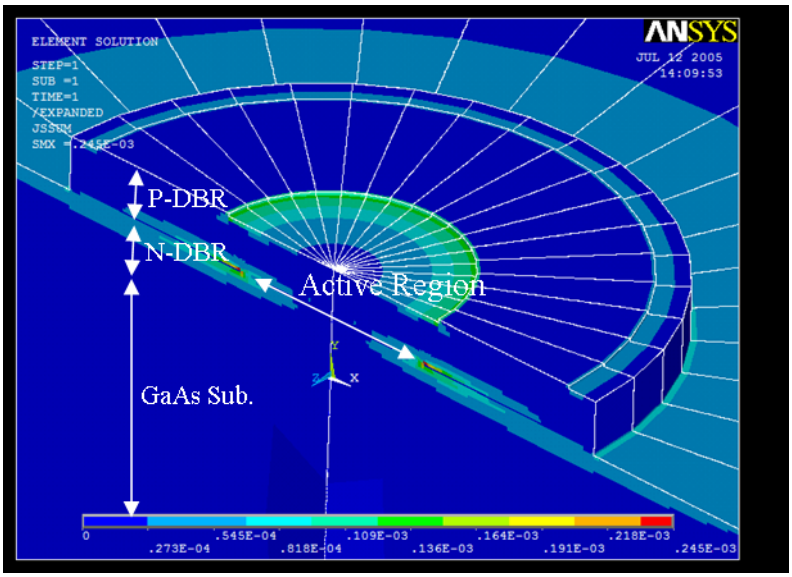


Figure 4-6 Current density distributions inside VCSEL near the active region

Calculated and experimentally measured thermal resistances are shown in Fig. 4-7 with ambient temperature set at 25 ^{o}C. Calculated thermal resistances as a function of substrate thickness of VCSEL are matched well with the experimentally measured results. This result shows that the simulation models for this study are properly carried out and thinned VCSEL has an exclusive advantage of heat management due to the reduction of the thermal resistance. Thermal resistance of 10 μm thick VCSEL is 40 % lower than that of 200 μm thick VCSEL. Calculated active region temperatures for 200 μm and 10 μm thick VCSEL are 47.16 ^{o}C and 38.9 ^{o}C, respectively.

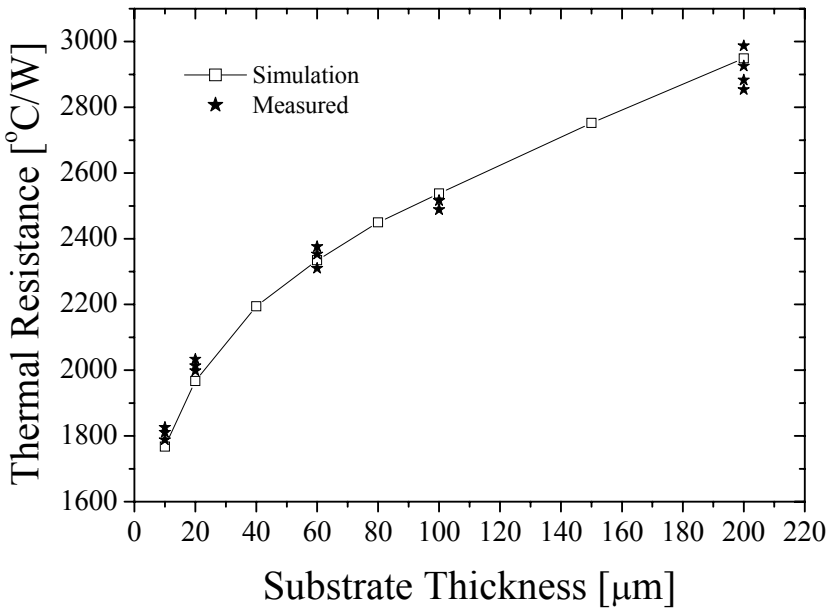


Figure 4-7 Simulation and experimental results of thermal resistances as a function of substrate thickness of thin film VCSEL

4.4. Thermal-Via Structures for the Fully Embedded Thin Film VCSEL

Thermally, via plays a significant role in locally enhancing the heat conduction through the board because the thermal conductivity of copper is 1200 times than that of common dielectric materials [54]. On the backside of the fully embedded thin film VCSEL, a thermal blind-via, where it enters one side and stop at an internal layer, will be applied as a heat sink structure. Fig. 4-8 (A) and (B) show simulation results of temperature distribution inside VCSEL with two commonly employed thermal via structures, the closed blind via (copper filled inside via hole-(A)) and the open blind via (30 μm thick copper electroplated inside via hole-(B)), respectively. In this simulation

model, we assumed the top of the VCSEL is covered by a polymer layer, which is the wave guiding layer as shown in ref [29, 31].

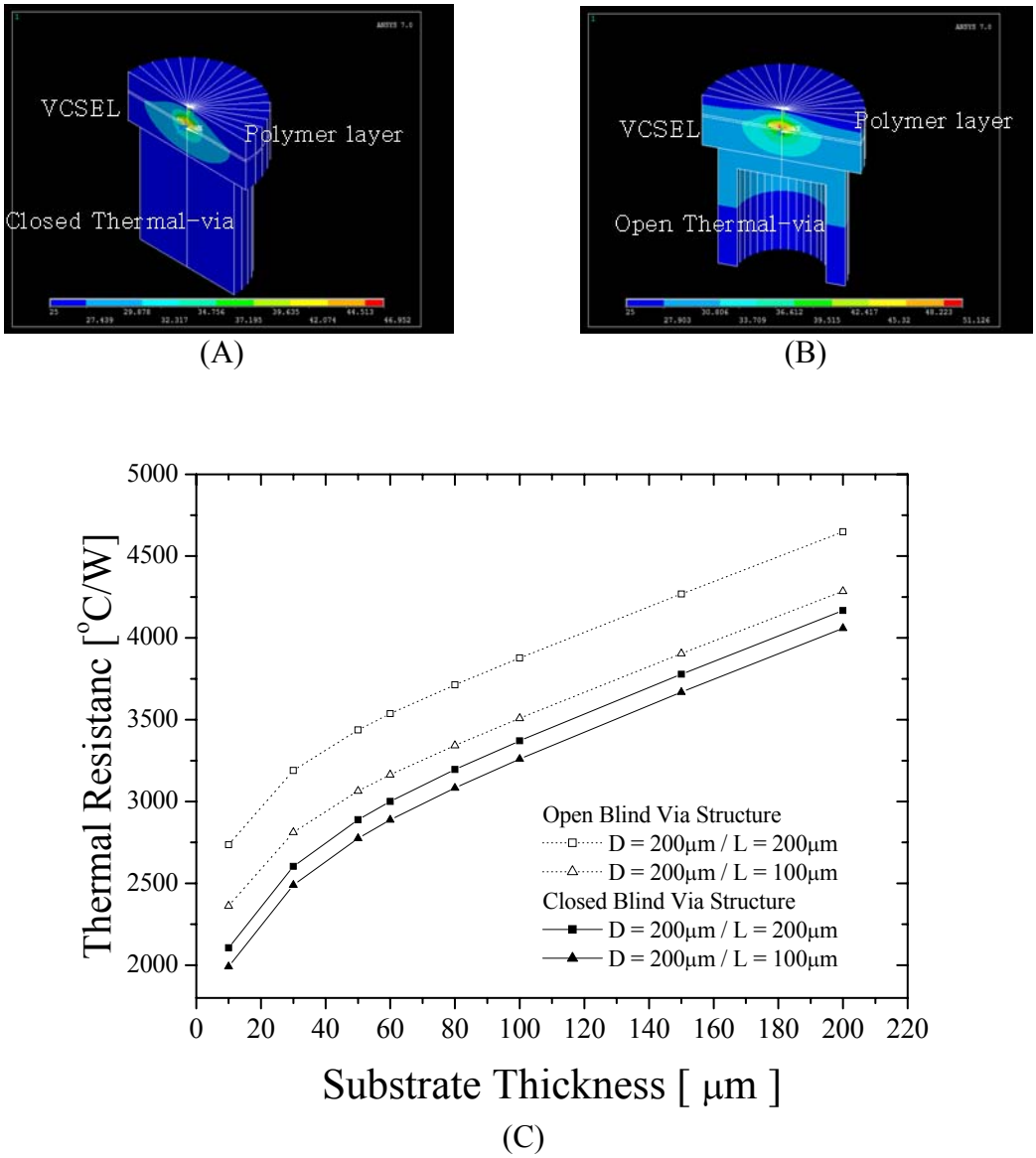


Figure 4-8 (A) Thin film VCSEL with a backside closed blind via structure, (B) Thin film VCSEL with a backside open blind via structure, (C) Simulation results of thermal resistance as a function of substrate thickness of thin film VCSEL with different thermal via structures

Fig. 4-8 (C) shows theoretically determined thermal resistances of the fully embedded thin film VCSEL with different thermal via structures. Following the previous results (Fig. 4-7), the compatible thermal resistance for the fully embedded VCSEL structure should be in the same range of 200 μm thick VCSEL with 25 ^{o}C substrate cooling condition. Therefore, in this study, the target thermal resistance is determined to be in the range of 2800 ~ 3000 ^{o}C/W. In the case of the open blind via structures (straight lines in Fig. 4-8(C)) with an aspect ratio of 1 and 0.5, the effective substrate thickness of thin film VCSEL is estimated to be in the range of 12 μm ~ 22 μm and 29 μm ~ 46 μm, respectively. Also, in the case of the closed blind via structures (dotted lines in Figure 8(C)) with an aspect ratio of 1 and 0.5, the fully embedded structure compatible substrate thickness of VCSEL is in the range of 44 μm ~ 60 μm and 53 μm ~ 72 μm, respectively. Fig. 4-9 shows a via hole structure on the optical film fabricated with a diameter of 200 μm and an aspect ratio of 0.5. The copper pillar inside via hole is clearly shown. Such a thermal via will be integrated according to the scheme shown in chapter 2.

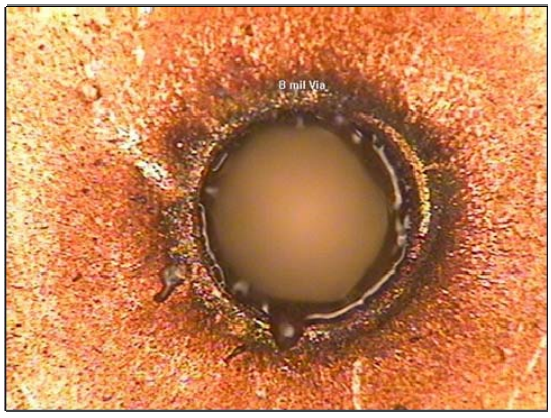


Figure 4-9 Fabricated via-hole on the optical film layer (D = 200 μm, Aspect ratio = 0.5)

4.5. Summary

The thermal resistances of substrate thinned VCSEL are experimentally measured and calculated using the 2-D thermal-electric coupled field analysis method. Both the joule heating and the non-radiative recombination effects are considered to calculate the heat source and the temperature rise distributions inside VCSEL near the active region. The thermal-electric analysis results matched well with experimental data. Simulation models for this study are properly carried out, and a thinned VCSEL had an exclusive advantage of the heat management. The thermal resistance of 10 μm thick VCSEL is 40 % lower than that of 200 μm thick VCSEL. According to the theoretical analysis of the thermal-via structures for fully embedded thin film VCSEL, calculated thin film VCSEL thickness compatible with the fully embedded board level optical interconnection system is depends on the thermal-via structures. In the case of the closed thermal via structures, the substrate thickness of VCSEL in the range of 44 μm ~ 72 μm is conformable in the fully embedded board level optical interconnection system.

Chapter 5: Design & Fabrication of 16-Channel Optical Backplane Bus with Volume Holographic Gratings

5.1. Multi-channels Optical Backplane Bus

Optical interconnection technology should become more important in the near future because the electrical interconnection is limited by speed and the difficulty of high integration density. At a high frequency operation (>10 GHz), copper transmission lines on PCB provoke degradation in the rise and fall times of electrical signals. Optical interconnection provides the potential for a higher data rate for each bus channel and the advantage of reduced transmission-line-related problems.

Optical backplane uses an optical signal to realize communications for board-to-board interconnection. Each board is equipped with optoelectronic converters (VCSELs and photodiodes) for the emission and detection of modulated optical signals. Several optical bus architectures based on the optical backplane have been proposed including the substrate-mode guided-wave bus system implemented with wave-guiding plates and holographic grating elements [33,34,35] and the free-space bus systems implemented through free-space optical interconnections [36,37].

In this chapter, a three-dimensionally interconnected 16-channel optical backplane is demonstrated for a high-performance computing system. As shown in Fig. 5-1, the optical backplane contains TO-46-CAN packaged VCSELs and photodiodes as an optical transmitter and receiver, respectively. Thin film volume holographic gratings are fabricated to refract light beams into a glass wave-guiding plate (refractive index

1.52) for total internal refraction. Through the VHOE (Volume Holographic Optical Elements), equalized fan-out beam intensities are experimentally measured.

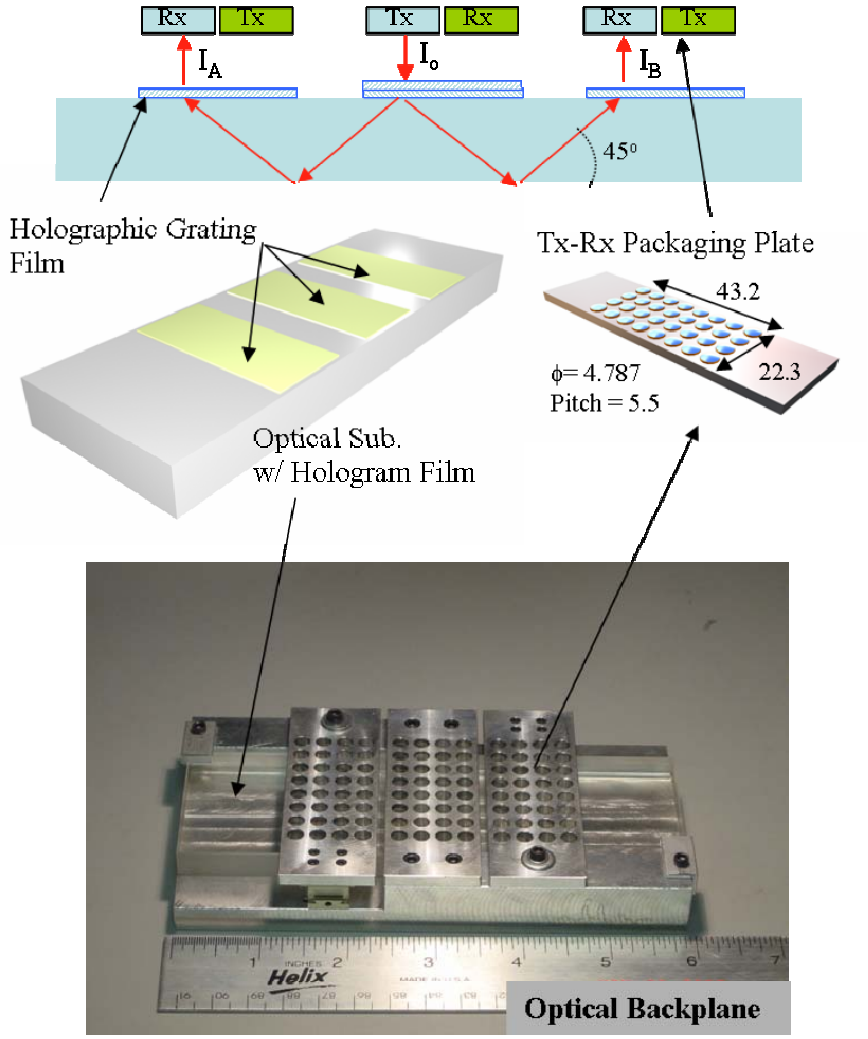


Figure 5-1 Schematic diagram of 16-channel optical backplane. (Optical signal redirection through thin film volume holographic gratings and a glass wave-guiding plate by total internal reflection)

Packaging issues including crosstalk and alignment tolerance are theoretically studied to design a low cost and simple optical packaging structure. A 4 X 8 optical packaging plate is fabricated to assemble 16-VCSELs and 16-Photodiodes. VCSELs and photodiodes are inserted alternatively into 32-holes drilled with a 4 X 8 row-and-column pattern as shown in Fig. 5-1. VCSEL driver ICs and TIAs (trans-impedance amplifiers) are integrated on the PC-board to control VCSEL and to amplify the electrical signal from photodiode, respectively. A 1.6 Gbps of data transmission rate (100 Mbps per single channel) is demonstrated through the optical backplane system using volume holographic gratings.

5.2. Fabrication of Volume Holographic Gratings and Optical Packaging Plate

The photopolymer-based volume hologram is an attractive option for making high-efficiency gratings. Single hologram gratings are recorded in DuPont photopolymer (HRF-600) films to refract input/output signal beams at 45^{o}. The film's thickness is 10 μm. The 532 nm wavelength Verdi laser was used for making all exposures. The film has little response at 850 nm, which allows *in situ* monitoring at this wavelength. The diffracted light from a 850 nm probe laser was monitored to measure the dynamic diffraction efficiency.

Measured diffraction efficiency variations of hologram film as a function of recording conditions are shown in Fig. 5-2. At the 1.5 W laser output power condition with dual beam power ratio 1:0.2, as-recorded diffraction efficiency of hologram grating

is saturated after 200 sec recording time. A maximum 65 ~ 70 % of diffraction efficiency is achieved after the post treatments, UV-curing (100 mJ/cm^2, 5 min) and heat-treatment (140 ^{o}C, 2 hr). 4 pieces of volume holographic films are recorded on the glass substrate as shown in Fig. 5-3.

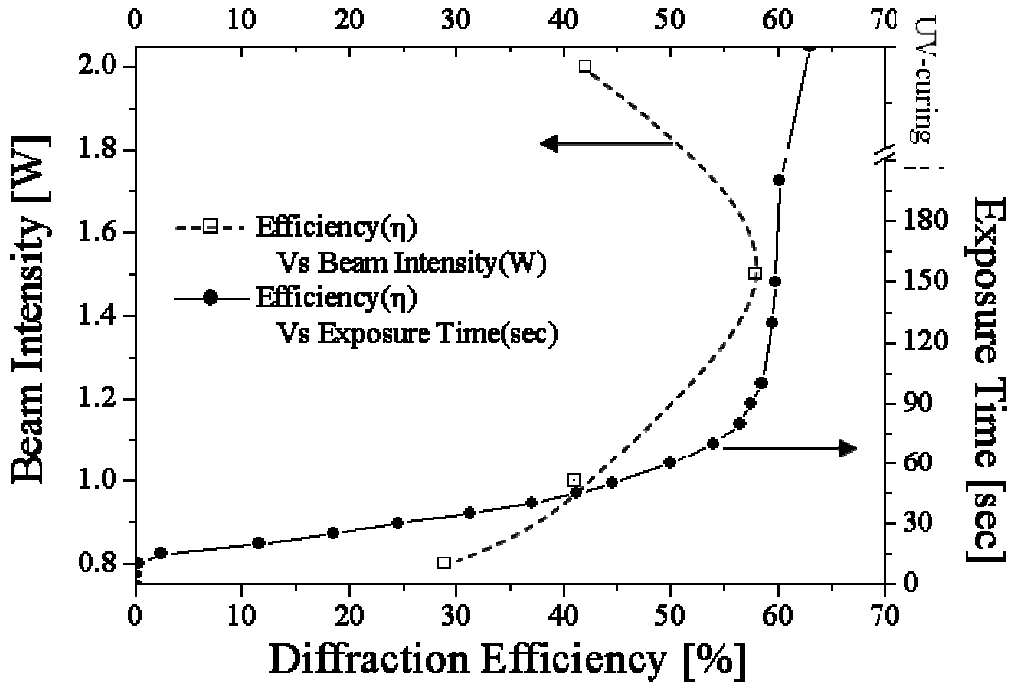


Figure 5-2 Diffracted efficiency variations as a function of hologram recording parameters [recording beam intensity and exposure time]

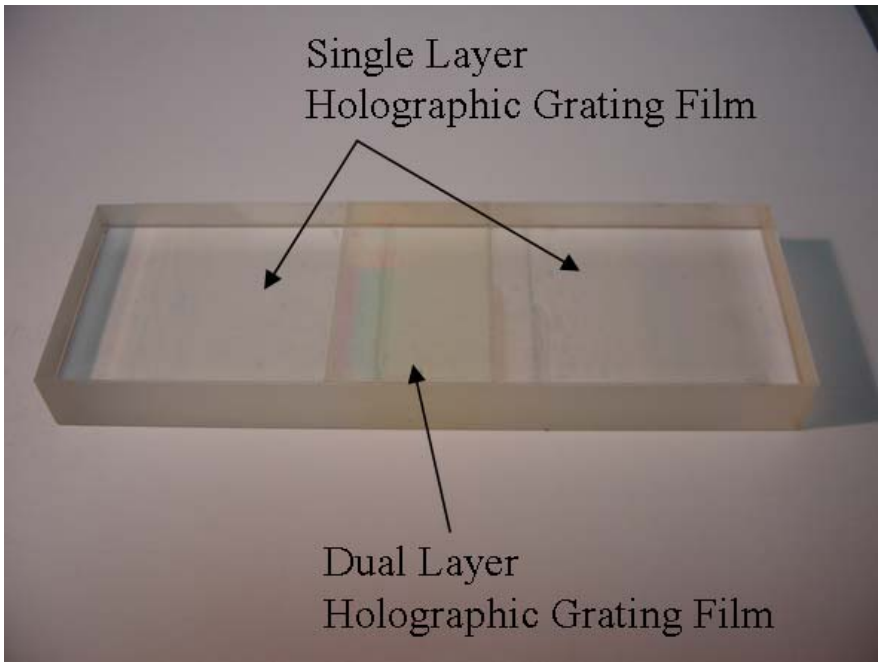


Figure 5-3 Recorded volume holographic films on the glass substrate [the size of holographic rating film: the center dual layer = 30 mm X 50 mm / the side single layer = 40 mm X 50 mm]

To reduce the output beam diverge angle of VCSEL and to converge the input beam of photodiode, an individual dome-lens installed TO-46-CAN packaged VCSEL and photodiodes are used in this study. Due to the optical crosstalk between the adjacent optical bus lines, the minimum pitch between two adjacent photodiodes must be determined according to the requirement of the optical signal-to-noise (SNR) ratio. Since commercial TO-46-CAN packaged VCSEL and photodiode have the same radius, the physical minimum pitch in 4 X 8 row-and-column pattern packaging is 4.77 mm.

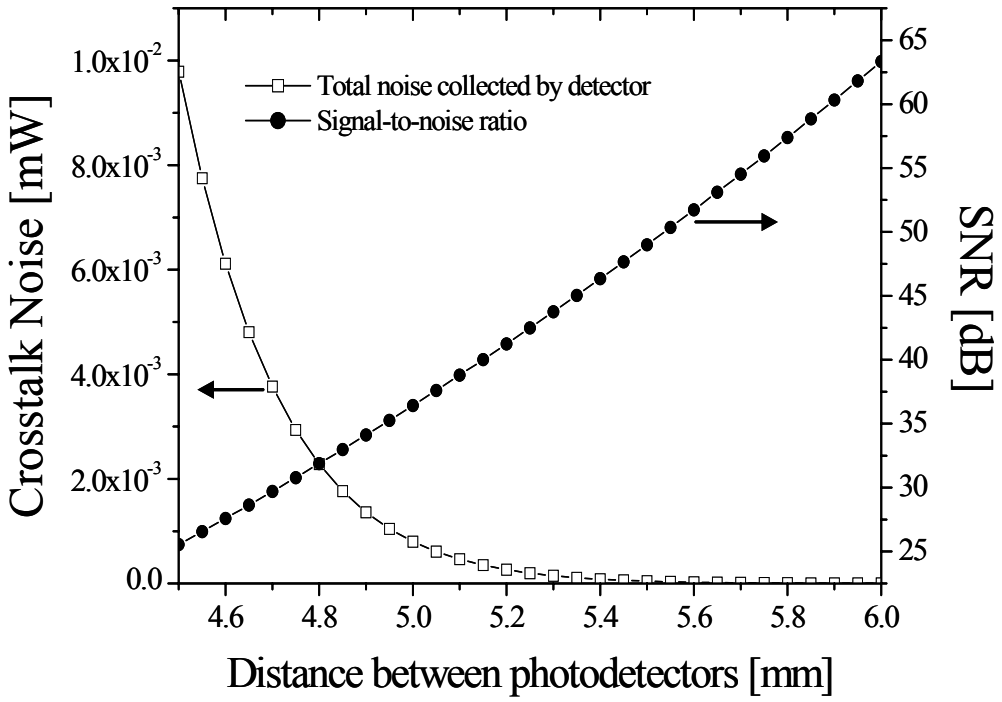


Figure 5-4 Calculated crosstalk and optical signal-to-noise ratio (SNR) as a function of photodiode pitch (with R = 2.38 mm) in the row and column pattern packaging plate

Fig. 5-4 shows that the calculated signal-to-noise ratio and crosstalk noise as a function of the distance between photo-detectors. As the pitch increases above 5 mm, crosstalk noise decreases and then disappeared below 1 μW. Also the geometrical optical path-length (30 mm) through VHOE and mechanical machining tolerances (± 0.25 μm) are considered in designing 4 X 8 row-and-column pattern packaging plates. In this study, 5.5 mm pitch optical packaging plates are fabricated. The distance between photodiodes after packaging, the diagonal distance in the row-and-column pattern, is 7.78 mm. Therefore, as based on Fig. 5-4, the optical crosstalk noise effect can be disregarded between two detectors in this packaging plate.

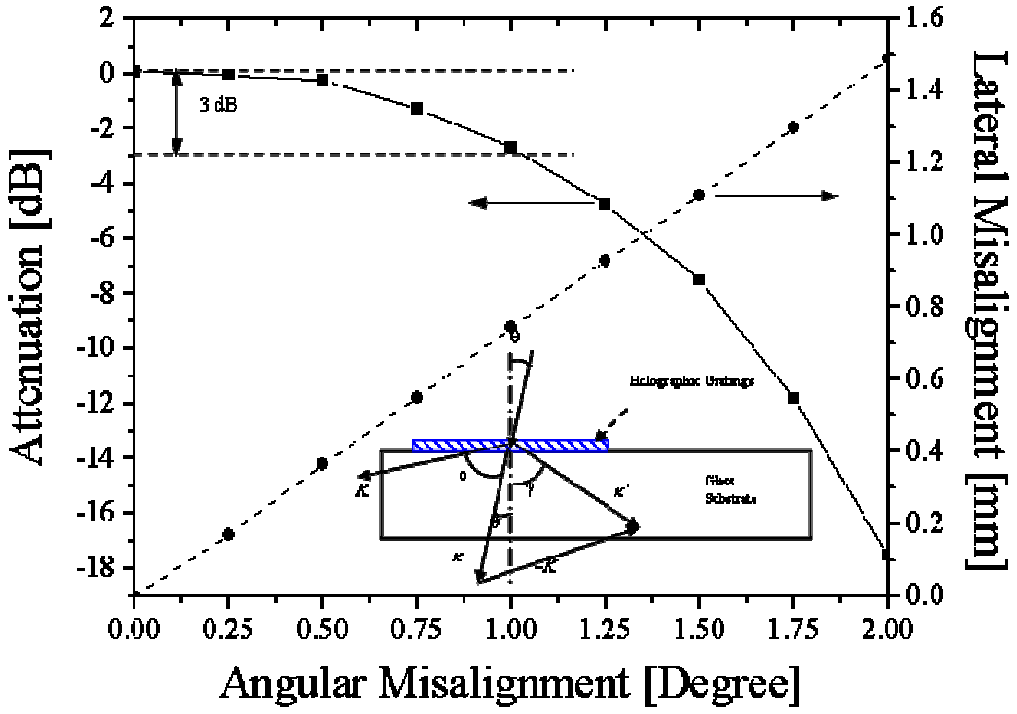


Figure 5-5 Measured fan-out power loss and calculated lateral misalignment (ΔL) as a function of input beam angular misalignment ($\Delta\theta$). (Inset Fig. 5-4: Phase-matching diagram correlating the grating vector K, the incident beam k, and the diffracted beam k` for a slanted holographic grating element)

The influence of angular misalignment on lateral misalignment arises from the phase mismatch between the input signal beam and the grating vector when the incident angle deviates from the Bragg angle. Inset of Fig. 5-5 shows the phase matching conditions of a volume holographic grating for surface-normal coupling.

For the Bragg condition, the relation between the incident angle and the diffracted angle is

$$\begin{pmatrix} -\sin\gamma \\ \cos\gamma \end{pmatrix} = \begin{pmatrix} \dfrac{\sin\theta}{n} - \dfrac{K}{\beta}\sin\phi \\ \left(1 - \dfrac{\sin^2\theta}{n^2} - \dfrac{K}{\beta}\cos\phi\right)^{1/2} \end{pmatrix} \tag{5-1}$$

where n is the refractive index of the hologram, $\beta(=2\pi n/\lambda)$ is the propagation constant of light with wavelength λ, and the meaning of γ, θ and K are as shown in inset of Fig. 5-5. After eliminating ϕ and differentiating the resulting equation, we have

$$\Delta\gamma = \frac{\left[\sin\theta - n\left(\dfrac{K^2}{2\beta^2} - 1\right)\sin\gamma\right]\cos\theta}{\left[\left(\dfrac{K^2}{2\beta^2} - 1\right)\sin\theta - n\sin\gamma\right]n\cos\gamma}\Delta\theta \tag{5-2}$$

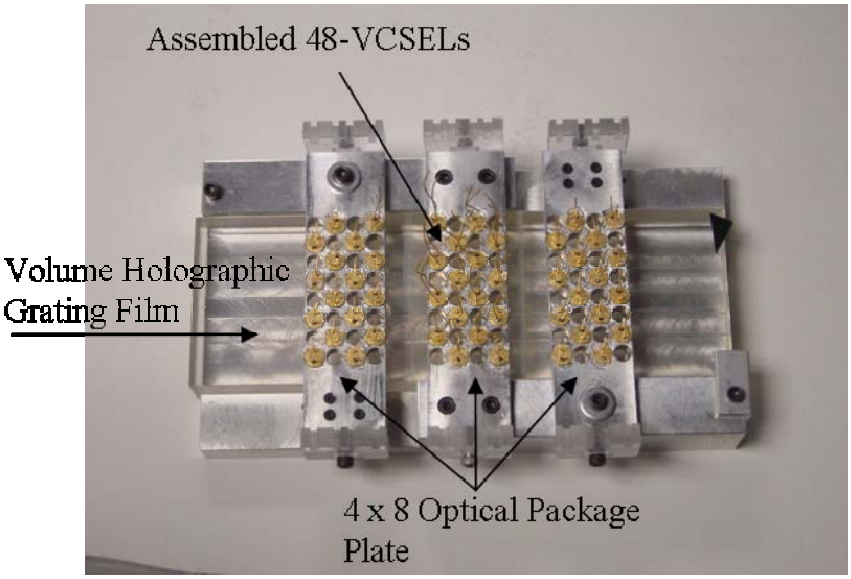
A variation of the angle of the input light beam leads to a spatial shift of the fan-out beam on the device surface of

$$\Delta L = \frac{\tan(\gamma + \Delta\gamma) - \tan\gamma}{\tan\gamma} \cdot L \tag{5-3}$$

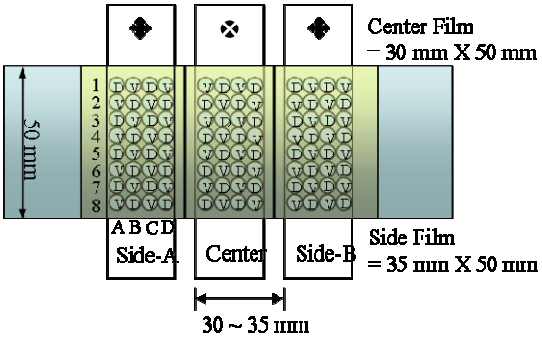
where, L is the distance between input and output beam positions.

Fig. 5-5 shows the calculated lateral deviation (ΔL) as a function of the incident angle ($\Delta\theta$) and measured fan-out power intensity variations as a function of in-put beam angular misalignment ($\Delta\theta$). Experimental results show that a 1° angular misalignment accompanied by 3dB fan-out power loss and it is related to a 0.76 mm lateral misalignment, concurrently. To obtain maximum fan-out power through VHOE, during VCSEL packaging, the angular misalignment is minimized below 1° and induced lateral

misalignment can be adjusted using a micro-stage assembled with an optical packaging plate as shown in Fig. 5-1.



(A)



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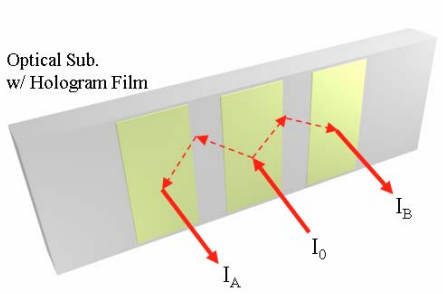


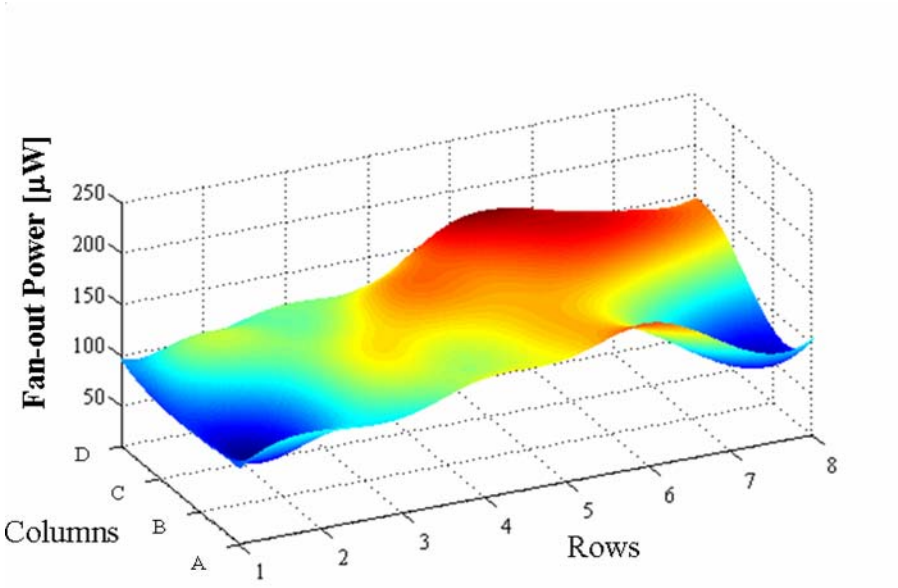
(C)

Figure 5-6 (A) 48-VCSELs assembled optical backplane system, (B) Schematic diagram of the row-and-column pattern packaging of 48-VCSELs and 48-detectors, (C) Schematic view of equalized fan-out beam directions through the volume holographic grating films

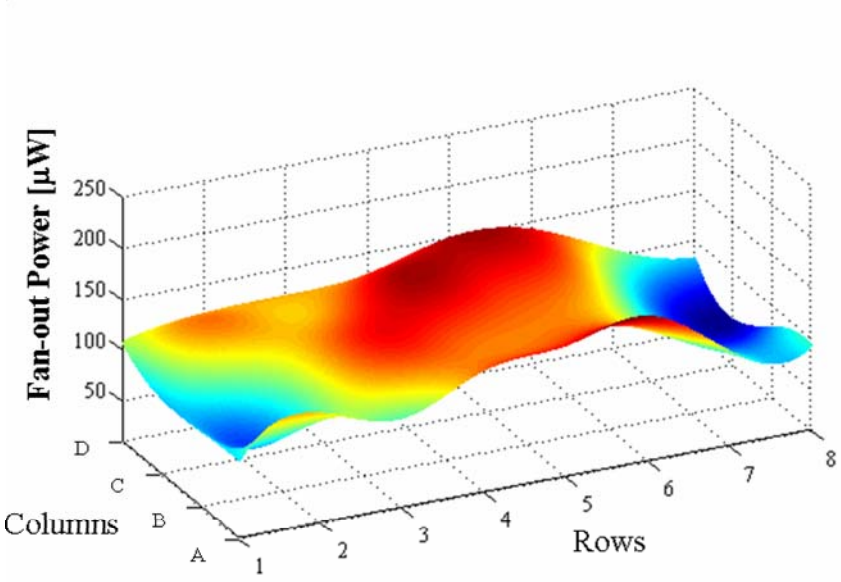
To optically interconnect 4 X 8 Tx-Rx arrays using VHOE as shown in Fig. 5-6, recorded volume holographic grating films are attached on the glass substrate. The optical input signal beams, vertical to the holographic film surface, are refracted at 45^{o} by slanted fringe structures of transmission volume holographic gratings. Due to the total internal reflection, coupled input beams are propagating through a glass wave-guiding plate and then coupled out by the matched holographic gratings.

In this study, the size of the hologram film on the center and the sides (A and B) are 50 X 30 mm^2 and 50 X 40 mm^2, respectively. Since fan-out beam intensity depends upon not only the diffraction efficiency of the hologram film but also the input beam incident angle as shown in Fig. 5-5, the uniformity of the fan-out beam intensity through VHOE is one of the critical issues in this system.

The measured surface area of a single hologram film, covering 4 X 8 packaging array, is 21.28 X 43.3 mm^2. A 2 mW (1.88 V / 11 mA) VCSEL beam is used as an input source (I_o). 32-point fan-out beam intensities (I_A and I_B) are measured using 4 X 8 packaging plates (4-columns and 8-rows) shown in Fig. 5-6. Experimentally measured 3-D fan-out beam intensity profiles are shown in Fig. 5-7. From the system power budget point of view, the fan-out beam intensities should be larger than the minimum value of photo-sensitivity, 20 μW, of photodiode with TIA. All fan-out beam intensity values through VHOE are in the range of 53.2 μW ~ 165.6 μW. The average intensity values in the center and the edge of holographic grating film are 135 μW and 80 μW, respectively.



(A)



(B)

Figure 5-7 Measured equalized fan-out power (I_A & I_B shown in Fig.4) uniformity through volume holographic grating films.(A) Equalized fan-out power distribution through $I_o \rightarrow I_A$, (B) Equalized fan-out power distribution through $I_o \rightarrow I_B$

Since 16-VCSELs and 16-photodiodes are alternatively packaged into 32 packaging holes (4 X 8 row-and-column pattern as shown in Fig. 5-1), 16-channel fan-out powers from the center plate to the sides (left and right), and vise versa, are measured.

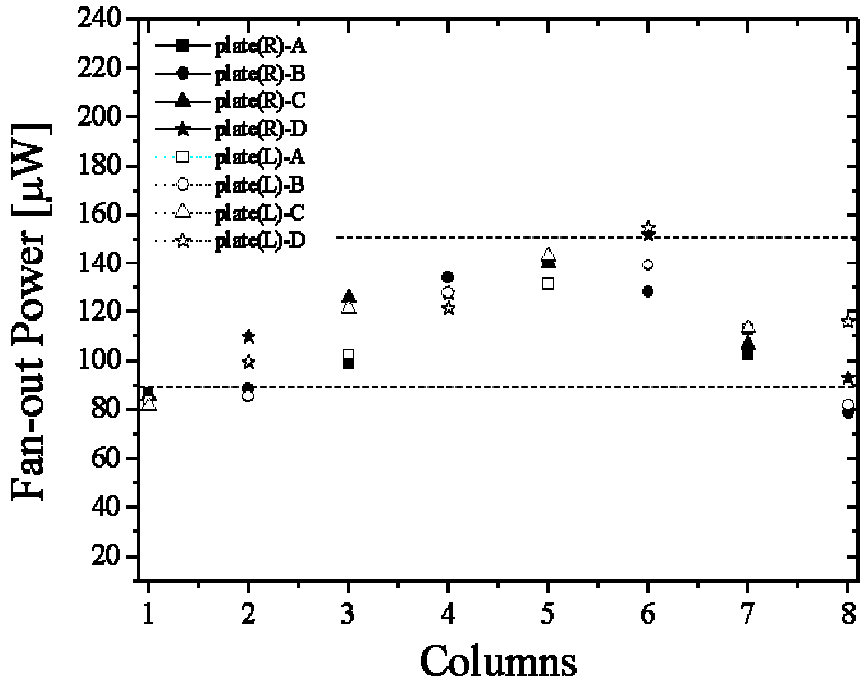


Figure 5-8 Measured 16-channels equalized fan-out powers (I_A & I_B shown in Fig.4) through VHOE [plate(R/L)-row, I_0 = 2 mW]

During VCSEL packaging, fan-out beam intensities are simultaneously monitored and the optimum packaging position is adjusted to achieve even fan-out power through VHOE. Fig. 5-8 shows that 90% of 16-channel fan-out beam intensities are in the range

of 90 μW ~ 150 μW. Moreover, the measured minimum fan-out power is 78.9 μW which is 5dB higher than the minimum power requirement of this system.

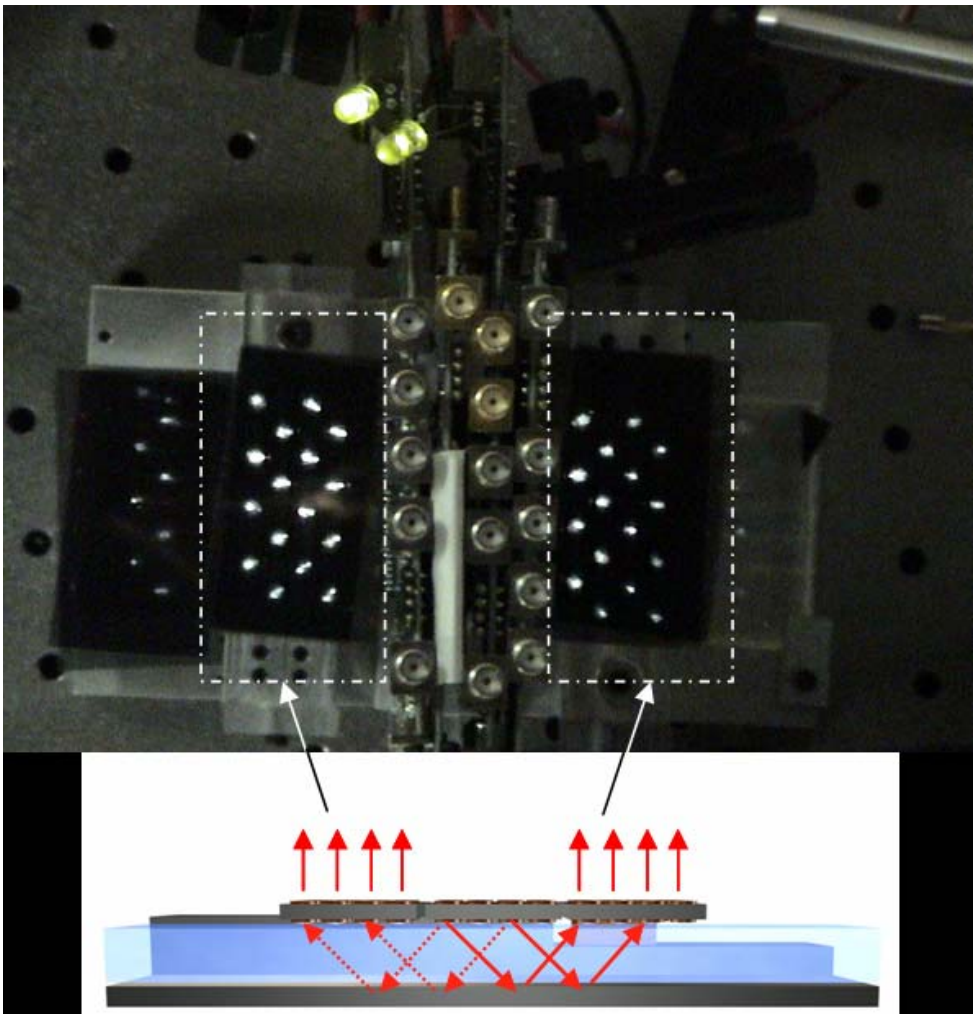


Figure 5-9 Measured far-field image of 16-channel equalized fan-out beam through VHOE [16 beam spots inside the box show the far-field images of 16 VCSEL beams diffracted by volume holographic optical elements (VHOE)]

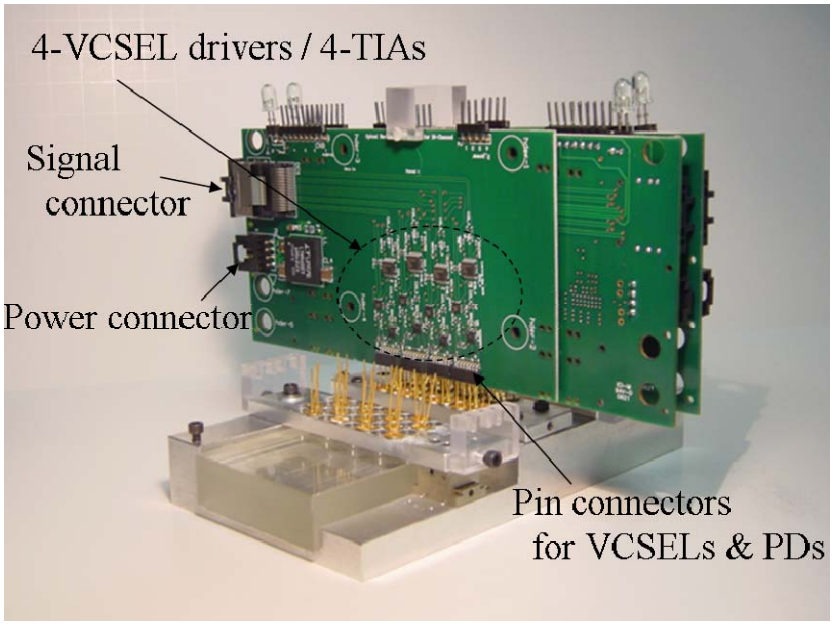
The far-field image of 16-channel equalized fan-out beam is measured by a CCD camera as shown in Fig. 5-9. Broadcasting 16-channel beam spots are clearly shown on

the both sides of package plate.

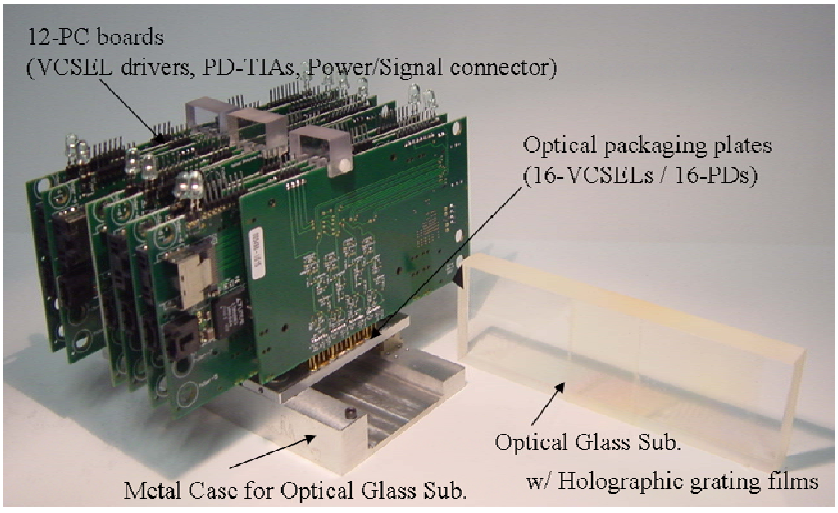
5.3. System Assemble and Performance Test

All optical components, VCSELs, Photodiodes and VHOE, are precisely assembled using optical packaging plates and the metal case structure shown in Fig. 5-10. The center packaging plate is physically bolted on the case. Two side packaging plates are designed to move laterally within a range of ±1.5 mm using micro-stage. In each optical plate, 16-VCSELs and 16-Photodiodes are arranged in row-and-column pattern as shown in Fig. 5-1.

Optical guided-wave glass plate with volume hologram films is also inserted into the case and then mechanically assembled. A total of 48-VCSELs and 48-PDs are precisely aligned and then packaged to get maximum fan-out power distributions as discussed in section 5.2. Electrical control boards are located on the top of the packaging plate as shown in Fig. 5-10. Each electrical board contains 4-VCSEL drivers and 4-PD-TIAs (trans-impedance amplifiers) alternatively. Four PC-boards are assembled on a single optical packaging plate to control the 16-VCSELs and 16-photodiodes. A total of 12 PC-boards are plugged to control 48-VCSELs and 48-photodetectors in this system.



(A)



(B)

Figure 5-10 Optical backplane system. (A) Assembled with PC-boards containing VCSEL drivers, PD-TIAs, power/signal connector and device pin connector, (B) Optical glass substrate and volume holographic grating films

Fig. 5-11 shows a single channel eye-diagram at 100 MHz measured by a digital communication analyzer (HP-83480A). The pulse pattern generator provides the modulation by generating a 2^{23}-1 pseudorandom bit sequence (PRBS) non return-to-zero (NRZ) pattern. Measured Jitter-RMS and Q-factor are 1.46ns and 51.18, respectively. Measured single channel eye-diagram shows reasonable opening at 100 MHz. All other channels are individually tested and optical connection performance between VCSEL and photodiode through VHOE is verified.

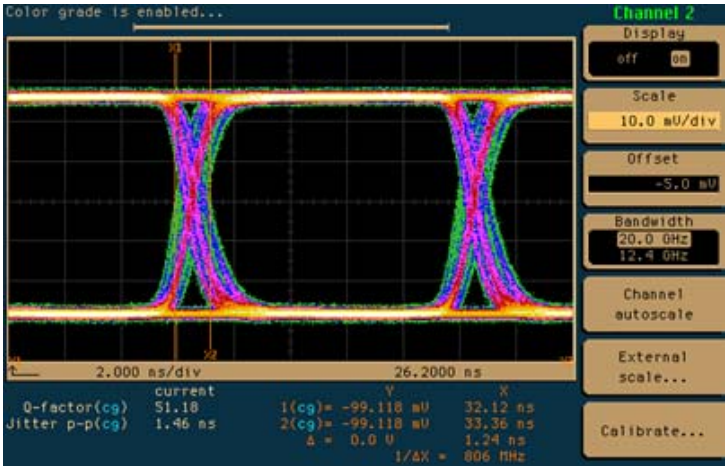


Figure 5-11 Single channel eye-diagram at 100 MHz through optical backplane system

All optical and electrical components are connected properly using cable connectors. The optical part (shown in Fig 5-8) consists of the hologram based optical backplane and 12-PC-boards containing VCSEL drivers, PD-TIAs, power connectors and signal connecters. The electrical part consists of two signal control boards and computing

modules to operate a high speed computing system. The high speed computing system demonstration is performed using the set-up shown in Fig. 5-12.

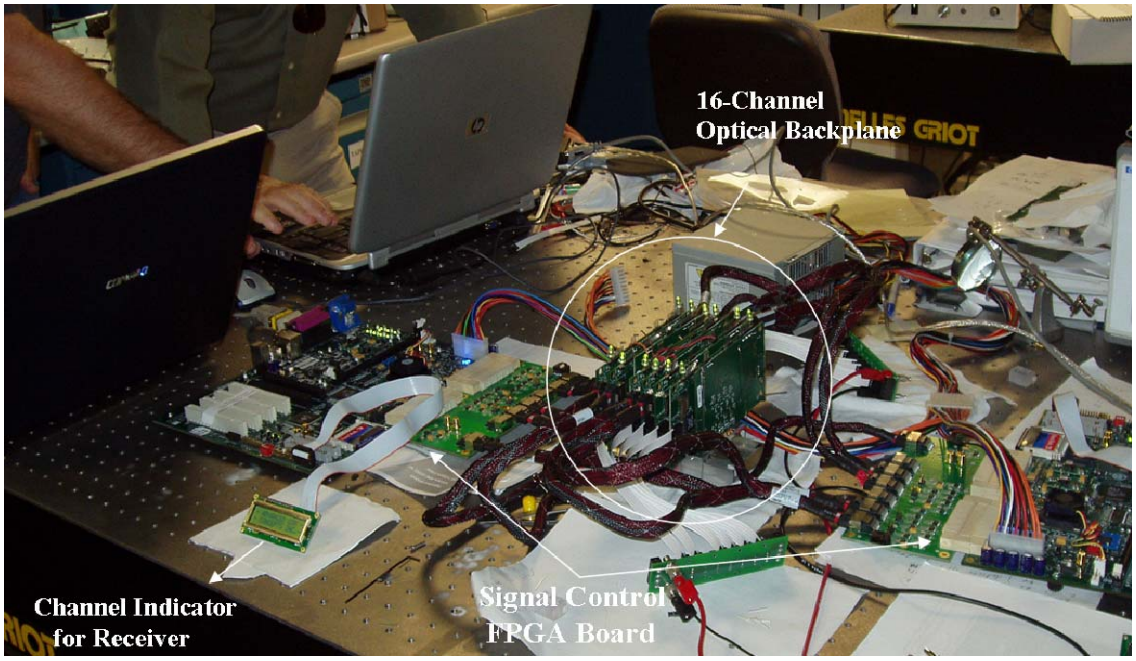


Figure 5-12 Demonstration setup for high speed computing system with 16-channel optical backplane bus (2 FPGA boards containing CUP and memories are controlled by lab-top computers, respectively. 16-channel optical backplane bus is connected between 2 FPGA boards to transfer data optically)

In this demonstration, the computing system controls two FPGA boards to monitor BER (Bit Error Rate) test using 10,000 date packet per single channel. All 16 channels are monitored simultaneously. BER test result shows no error data transfer through the 16-channel optical backplane bus with VHOE. Total 64 channels including 32 broadcasting channels are successfully demonstrated with the commercial computing system.

5.4. Summary

A novel 16-channel optical backplane bus using thin film volume holographic gratings is designed and fabricated to demonstrate 1.6 Gbps of data transmission (100Mbps per single channel). Thin film volume holographic gratings are fabricated to refract light beams into a glass wave-guiding plate (refractive index 1.52) for total internal refraction. Through the VHOE (Volume Holographic Optical Elements), equalized fan-out beam intensities are experimentally measured. Packaging issues including crosstalk and alignment tolerance are theoretically studied to design a low cost and simple optical packaging structure. A 4 X 8 optical packaging plate is fabricated to assemble 16-VCSELs and 16-Photodiodes. VCSELs and photodiodes are inserted alternatively into 32-holes drilled with a 4 X 8 row-and-column pattern optical packaging plate. 16-channel fan-out beam intensities are in the range of 90 μW ~ 150 μW. Moreover, the measured minimum fan-out power is 78.9 μW which is 5dB higher than the minimum power requirement of this system. A 1.6 Gbps of data transmission rate (100 Mbps per single channel) is demonstrated through the optical backplane system using volume holographic gratings. In this study, the target data transmission rate of VHOE backplane system is 1.6 Gbps, 16 channels at 100 MHz per channel. VHOE backplanes can be expected to support Terabit data rates in inexpensive, mechanically robust and reliable form factors.

Chapter 6: Conclusions

The thin film VCSEL and PIN photodiode arrays are fabricated by substrate thinning processes. In the point of view of device damage during handling, the range of thickness between 50 μm and 80 μm is compatible for the fully embedded structure. Also the thermal effects of thin film VCSEL are studied to verify optimum thickness of VCSEL for the fully embedded structure. The thermal resistances of substrate thinned VCSEL are experimentally measured and calculated using the 2-D thermal-electric coupled field analysis method. Both the joule heating and the non-radiative recombination effects are considered to calculate the heat source and the temperature rise distributions inside VCSEL near the active region. The thermal-electric analysis results matched well with experimental data. Simulation models for this study are properly carried out, and a thinned VCSEL had an exclusive advantage of the heat management. The thermal resistance of 10 μm thick VCSEL is 40 % lower than that of 200 μm thick VCSEL. Calculated active region temperatures for 200 μm and 10 μm thick VCSEL are 47.16 ^{o}C and 38.9 ^{o}C, respectively. According to the theoretical analysis of the thermal-via structures for fully embedded thin film VCSEL, calculated thin film VCSEL thickness compatible with the fully embedded board level optical interconnection system is depends on the thermal-via structures. In the case of the closed thermal via structures, the substrate thickness of VCSEL in the range of 44 μm ~ 72 μm is conformable in the fully embedded board level optical interconnection system. This research is supported by Darpa, ONR and Texas ATP program.

A novel 16-channel optical backplane bus using thin film volume holographic gratings is fabricated to demonstrate a high-performance computing system. 16-channel optical backplane bus contains TO-46-CAN packaged VCSELs and photodiodes are used as an optical transmitter and receiver, respectively. Packaging issues including crosstalk and alignment tolerance are studied and a noble 4 X 8 optical packaging plate is designed for aligning VCSELs and Photodiodes. Volume holographic grating films are fabricated on a glass substrate to redirect I/O signal beams. Using VHOE (volume holographic optical elements), all 16-channel fan-out beam intensities are in the uniform range of 90 μW ~ 150 μW. Experimentally measured minimum equalized fan-out power is ~ 5dB higher than the minimum power requirement of this system. High performance computing system demonstrates 1.6 Gbps of data transmission (100Mbps per single channel) through optical backplane system using volume holographic gratings. In this study, VHOE backplane bus is verified to support 1.6 Gbps data rates in inexpensive, mechanically robust and reliable form factors.

10 Gbps high-speed electrical backplane demonstration is performed by Sinsky *et al.* [54]. A bit error rate (BER) less than 10^{-13} is achieved over an 87 cm transmission line using duobinary signal encoding. Recently, data transmission at 25 Gbps over a 61 cm link (15.25 Gbps·m) on an electrical backplane was demonstrated by the same group [55]. It is believed that the electrical backplane can support 100 Gbps Ethernet applications using conventional backplane design techniques (four channels at 25 Gb/s). However, a drawback of the approach so far is the high signal loss over the link of −50 dB at 25 GHz due to skin effects and dielectric losses in the FR4 material [56].

The future work of the novel optical backplane bus research is increase data rate up to 1.3 Tbps using 128 channels and 10.1 Gbps per individual channel. This research is supported by ACC.

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Vita

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